Preliminary

128K x 36 & 256K x 18 Late Write Synchronous Fast SRAM with Pipelined Data Output

Document Title

128K x 36 & 256K x 18 Late Write Synchronous Fast SRAM with Pipelined Data Output

Revision History

Rev. No.	History	Issue Date	Remark
2.0	Add JTAG standard	February 12, 1999	Preliminary

A65H73361/A65H83181 Series

128K x 36 & 256K x 18 Late Write Synchronous Fast SRAM with Pipelined Data Output

Preliminary

Features

- Fast access times: 2.5/3.0/3.5ns
- 128k x 36 or 256k x 18 organizations
- CMOS technology
- Register to register synchronous operation with self-timed late write
- Single +3.3V ±5% power supply
- Individual byte write and global write
- HSTL input & output levels
- Boundary scan(JTAG) IEEE 1149.1 compatible
- Asynchronous output enable
- Sleep mode (ZZ)
- Programmable impedance output drivers
- JEDEC Standard pinout and boundary scan order
- 7 x 17 bump plastic ball grid array (PBGA) package

General Description

The A65H73361 and A65H83181 are 128k words by 36 bits and 256k words by 18 bits late write synchronous 4Mb SRAMS built using high performance CMOS process.

The differential clock are used to control the timing of read/write operation and all internal operations are self-timed. The positive edge triggered CK clock input controls all addresses write-enables and Synchronous select and data ins are registered.

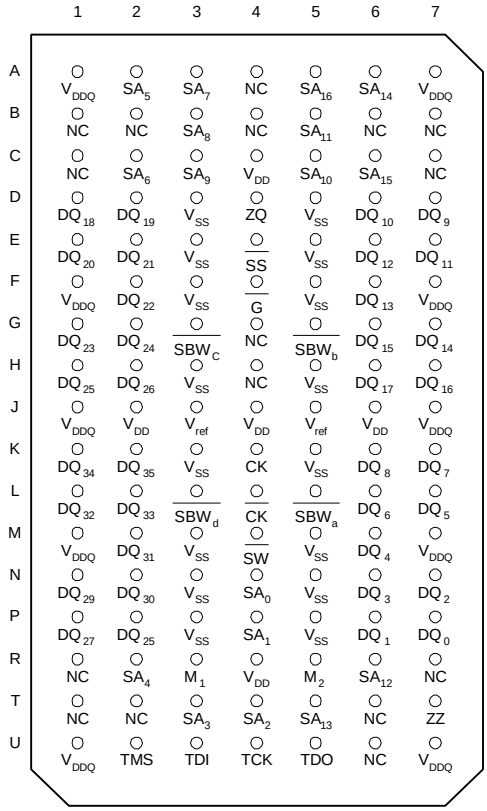
The data outs are controlled by the output registers off the next positive clock edge to be updated.

The internal write buffer enables write data to be accepted on the rising edge of the clock one cycle after address and control signals.

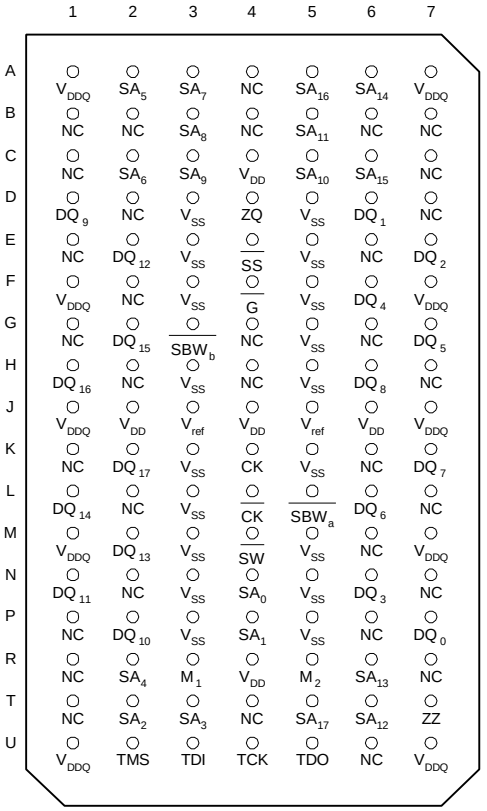
The SRAM uses HSTL I/O interfaces with programmable impedance output drivers allowing the outputs to match the impedance of the circuit traces which reduces signal reflections.

Pin Configuration

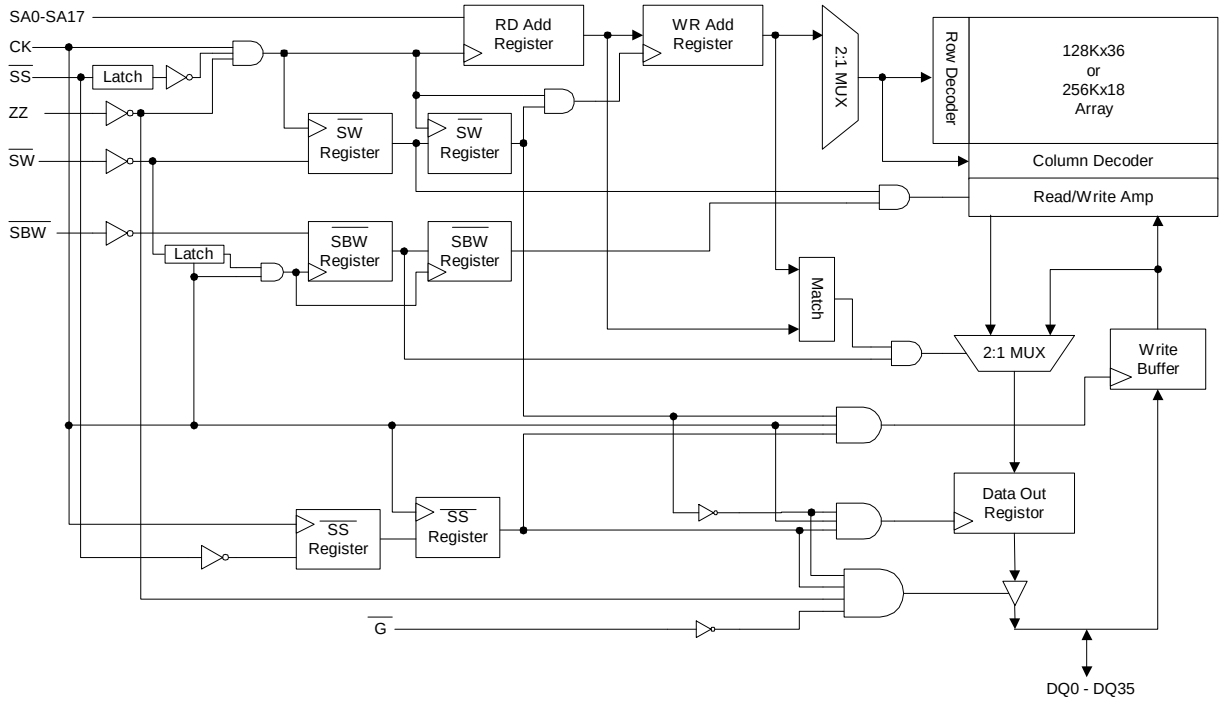
A65H73361



A65H83181



Block Diagram



Pin Description

SA0-SA17	Address input (X18 : SA0 - SA17, X36 : SA0 - SA16)	$\overline{G}$	Asynchronous output enable
DQ0-DQ35	Data I/O (X18 : DQ0 - DQ17, X36 : DQ0 - DQ35)	$\overline{SS}$	Synchronous select
CK , $\overline{CK}$	Differential input register clocks	M1, M2	For boundary scan purpose
$\overline{SW}$	Write enable. Global	V_{REP}(2)	HSTL input reference voltage
$\overline{SBWa}$	Write enable. Byte a (DQ0-DQ8)	V_{DD}	Power supply (+3.3V)
$\overline{SBWb}$	Write enable. Byte b (DQ9-DQ17)	V_{SS}	Ground
$\overline{SBWc}$	Write enable. Byte c (DQ18-DQ26)	V_{DDQ}	Output power supply
$\overline{SBWd}$	Write enable. Byte d (DQ27-DQ35)	ZZ	Asynchronous sleep mode
TMS, TDI, TCK	IEEE 1149.1 test inputs(LVTTL levels)	ZQ	Output driver impedance control
TDO	IEEE 1149.1 test output(LVTTL level)	NC	No connect

Clock Truth Table

K	ZZ	$\overline{SS}$	$\overline{SW}$	$\overline{SBWa}$	$\overline{SBWb}$	$\overline{SBWc}$	$\overline{SBWd}$	DQ(n)	DQ(n+1)	MODE
L→H	L	L	H	X	X	X	X	X	D_{OUT} 0-35	Read Cycle ALL Bytes
L→H	L	L	L	L	H	H	H	X	D_{IN} 0-8	Write Cycle 1st Byte
L→H	L	L	L	H	L	H	H	X	D_{IN} 9-17	Write Cycle 2nd Byte
L→H	L	L	L	H	H	L	H	X	D_{IN} 18-26	Write Cycle 3rd Byte
L→H	L	L	L	H	H	H	L	X	D_{IN} 27-35	Write Cycle 4th Byte
L→H	L	L	L	L	L	L	L	X	D_{IN} 0-35	Write Cycle ALL Byte
L→H	L	L	L	H	H	H	H	X	High-Z	Abort Write Cycle
L→H	L	H	X	X	X	X	X	X	High-Z	Deselect Cycle
X	H	X	X	X	X	X	X	High-Z	High-Z	Sleep Mode

Clock Truth Table

Operation	$\overline{G}$	DQ
Read	L	D_{OUT} 0-35
Read	H	High-Z
Sleep(ZZ=H)	X	High-Z
Write($\overline{SW}$ =L)	X	D_{IN}
Deselect($\overline{SS}$=H)	X	High-Z

Absolute Maximum Ratings*

Power Supply Voltage(V_{DD}) . . . . . -0.5V to +4.6V
Voltage Relative to GND for any Pin Except V_{DD}(V_{IN}, V_{OUT}) 0.5V
Power Dissipation (P_D) 1.0W
Operating Temperature (Topr). . . . . 0°C to 70°C
Storage Temperature (Tbias) . . . . . -10°C to 85°C
Storage Temperature(Tstg). . . . . .-55°C to 125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure the absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (T_J = 0 to 110°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	V_{DD}	3.15	3.3	3.47	V	1
Output Driver Supply Voltage	V_{DDQ}	1.4	1.5	1.6	V	1
Input High Voltage	V_{IH}	V_{REF}+0.1	-	V_{DDQ}+0.3	V	1, 2
Input Low Voltage	V_{IL}	-0.3	-	V_{REF}-0.1	V	1, 3
Input reference Voltage	V_{REF}	0.68	0.75	0.90	V	1, 6
Clocks Signal Voltage	V_{IN-CLK}	-0.3	-	V_{DDQ}+0.3	V	1, 4
Differential Clocks Signal Voltage	$V_{DIF-CLK}$	0.1	-	V_{DDQ}+0.6	V	1, 5
Clocks Common Mode Voltage	V_{CM-CLK}	0.55	-	0.90	V	1
Output Current	I_{OUT}	-	5	8	mA	

1.All voltage reference to V_{SS}. All V_{DD} V_{DDQ} and V_{SS} pins must be connected.
2.V_{IH}(Max)DC = V_{DD} + 0.3V, V_{IH}(Max)AC = V_{DD} + 1.5V (pulse width ≤ 4.0ns).
3.V_{IL}(Min)DC = -0.3V, V_{IL}(Min)AC = -1.5 V (pulse width ≤ 4.0ns).
4.V_{IN-CLK} specifies the maximum allowable DC excursions of each differential clock (CK , $\overline{CK}$).
5.$V_{DIF-CLK}$ specifies the minimum clock differential voltage required for switching.
6.Peak to Peak AC component superimposed on V_{REF} may not exceed 5% of V_{REF}.

DC Electrical Characteristics (T_J = 0 to +110°C, V_{DD} = 3.3V ± 5%)

Parameter	Symbol	Min.	Max.	Units	Notes
Average Power Supply Operating Current-X36 (I_{OUT} = 0, V_{IN} = V_{IH} or V_{IL}, ZZ & $\overline{SS}$ = V_{IL})	I_{DD5} I_{DD6} I_{DD7}	- -	TBD	mA	1
Average Power Supply Operating Current-X18 (I_{OUT} = 0, V_{IN} = V_{IH} or V_{IL}, ZZ & $\overline{SS}$ = V_{IL})	I_{DD5} I_{DD6} I_{DD7}	- -	TBD	mA	1
Power Supply Standby Current (ZZ = V_{IH}, All other inputs = V_{IH} or V_{IL}, I_{out} =0) ($\overline{SS}$ = V_{IH}, ZZ = V_{IL}. All their inputs = V_{IH} or V_{IL}, I_{OUT} = 0)	L_{sbzz} I_{SBss}	- -	TBD	mA mA	1 1
Input Leakage Current (V_{IN} = V_{SS} or V_{DD})	I_{LI}	-	±1.0	µA	
Output Leakage Current (V_{OUT} = V_{SS} or V_{DD}, DQ in High = Z)	I_{LO}	-	±1.0	µA	
Output High Level Voltage(I_{OH} = -6mA @ $V_{DDQ}/2_{+0.3}$)	V_{OH}	V_{DDQ}-.4	V_{DDQ}	V	2
Output Low Level Voltage(I_{OL} = +6mA @ $V_{DDQ}/2_{-0.3}$)	V_{OL}	V_{SS}	V_{SS}+.4	V	2

1. I_{OUT} = Chip Output Current.
2.Minimum Impedance Output Driver.

Capacitance (T_J = 0 to +110°C, V_{DD} = 3.3V ± 5%, f = 1MHz)

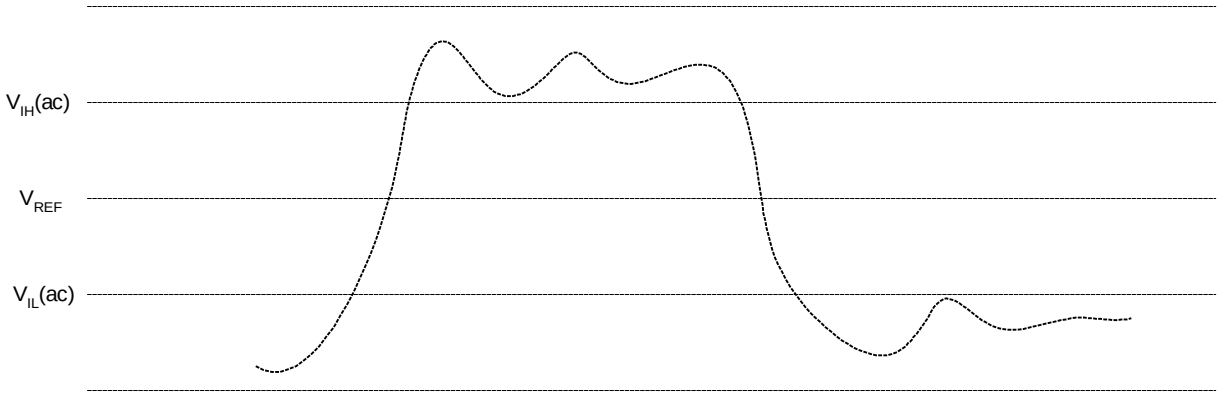
Parameter	Symbol	Test Condition	Max.	Units
Input Capacitance	C_{IN}	V_{IN} = 0V	3	pF
Data I/O Capacitance (DQ0-DQ35)	C_{OUT}	V_{OUT}= 0V	4	pF

AC Input Characteristics

Item	Symbol	Min.	Max.	Notes
AC Input Logic High	V_{IN} (ac)	TBD		3
AC Input Logic Low	V_{IL} (ac)		TBD	3
Clock Input Differential Voltage	V_{DIF} (ac)	TBD		2
V_{REF} Peak to Peak ac Voltage	V_{REF} (ac)		5% V_{REF} (dc)	1

1.The peak to peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF}.
2.Performance is a function on V_{IH} and V_{IL} levels to clock inputs.
3.See AC input Definition figure on page 7.

AC Input Definition



Programmable Impedance Output Driver DC Electrical Characteristics
(T_J = 0 to +110°C, V_{DD} = 3.3V ± 5%)

Parameter	Symbol	Min.	Max.	Units	Notes
Output High Level Voltage	V_{OH}	$V_{DDQ}/2$	V_{DDQ}	V	1
Output Low Level Voltage	V_{OL}	V_{SS}	$V_{DDQ}/2$	V	2

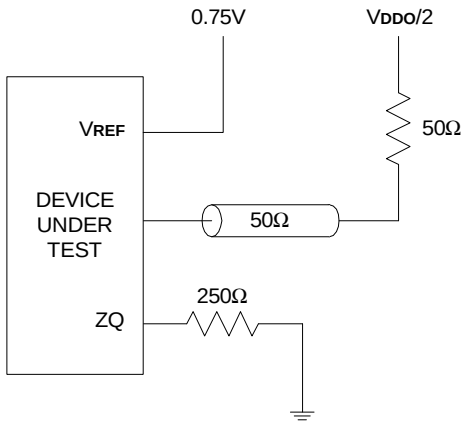
1.I_{OH} = (V_{DDQ}/2)/(RQ/5) 7.5% @ V_{OH} = V_{DDQ}/2 For :150Ω ≤ RQ ≤ 350Ω
2.I_{OL} = (V_{DDQ}/2)/(RQ/5) 7.5% @ V_{OL} = V_{DDQ}/2 For :150Ω ≤ RQ ≤ 350Ω

AC Test Conditions (T_J = 0 to +110°C, V_{DD} = 3.3V ± 5%, V_{DDQ} = 1.5V)

Parameter	Symbol	Conditions	units	Notes
Output High Level Voltage	V_{IH}	1.25	V	
Output Low Level Voltage	V_{IL}	0.25	V	
Input Reference Voltage	V_{REF}	0.75	V	
Differential Clocks Voltage	$V_{DIF-CLK}$	0.75	V	
Input Rise Time	T_R	0.5	ns	
Input Fall Time	T_F	0.5	ns	
I/O Signals Reference Level		0.75	V	
Clocks Reference level		Differential Cross Point	V	
Output Load Conditions				1

1.See AC Test Loading figure on page 8.

AC Test Loading

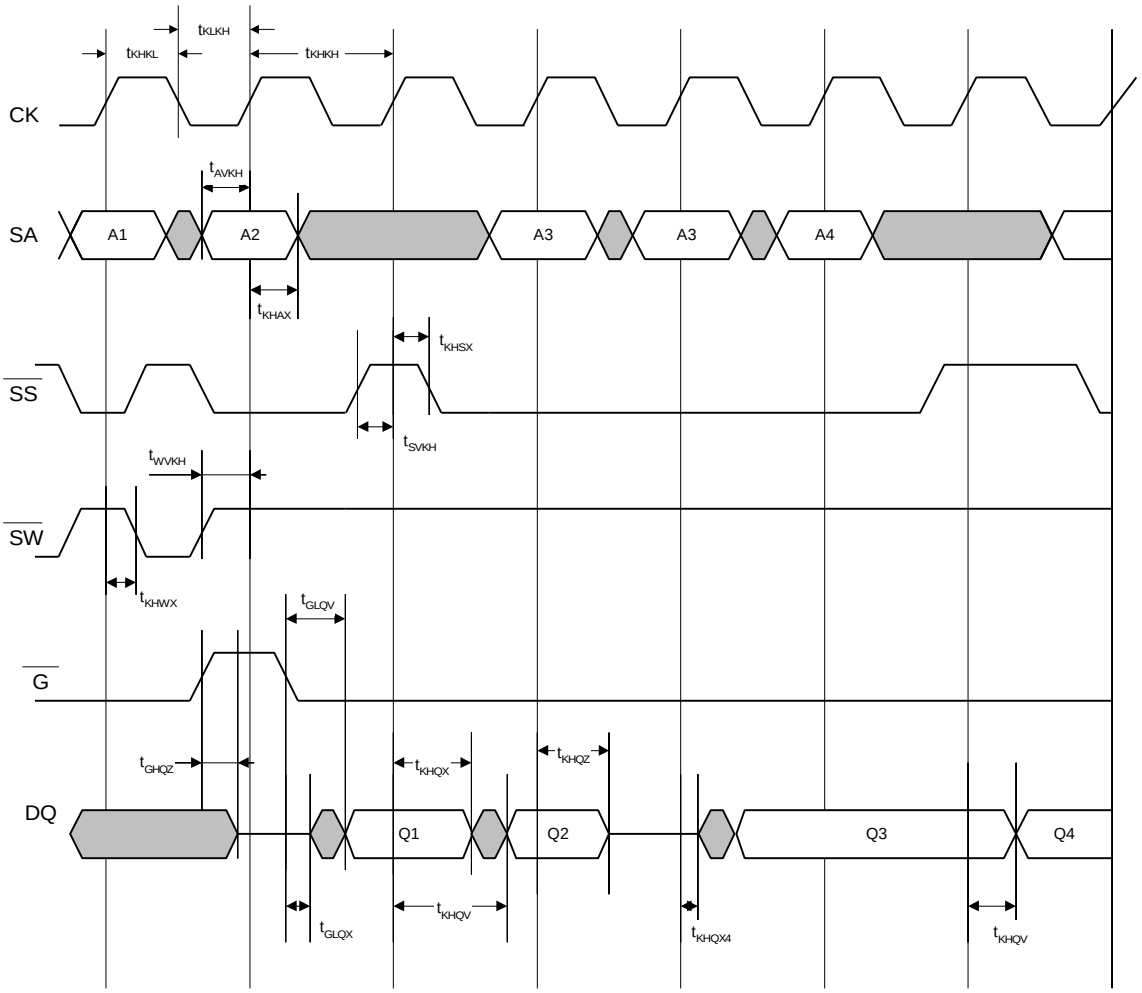


AC Characteristics (T_J = 0 to +110°C, V_{DD} = 3.3V ± 5%)

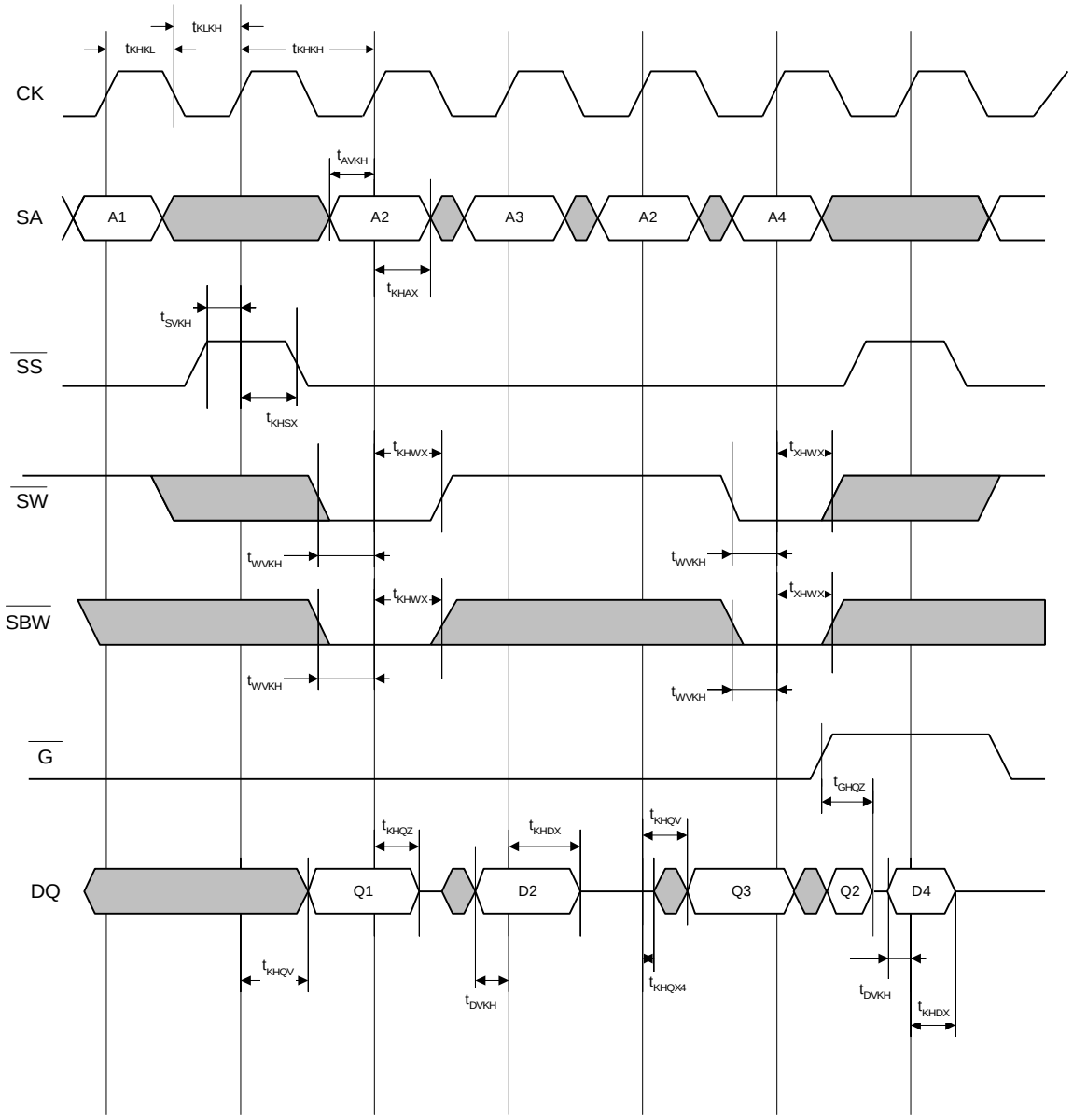
Parameter	Symbol	-5		-6		-7		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Cycle Time	t_{KHKH}	5	-	6.0	-	7.0	-	ns	
Clock High Pulse Width	t_{KHKL}	1.5	-	1.5	-	1.5	-	ns	
Clock Low Pulse Width	t_{KLKH}	1.5	-	1.5	-	1.5	-	ns	
Clock to Output Valid	t_{KHQV}	-	2.5		3.0	-	3.5	ns	1
Address Setup Time	t_{AVKH}	0.5	-	0.5	-	0.5	-	ns	4
Address Hold Time	t_{KHAX}	1.0	-	1.0	-	1.0	-	ns	4
Sync Select Setup Time	t_{SVKH}	0.5	-	0.5	-	0.5	-	ns	4
Sync Select Hold Time	t_{KHSX}	1.0	-	1.0	-	1.0	-	ns	4
Write Enables Setup Time	t_{WVKH}	0.5	-	0.5	-	0.5	-	ns	4
Write Enables Hold Time	t_{KHWX}	1.0	-	1.0	-	1.0	-	ns	4
Data In Setup Time	t_{DVKH}	0.5	-	0.5	-	0.5	-	ns	4
Data In Hold Time	t_{KHDX}	1.0	-	1.0	-	1.0	-	ns	4
Data Out Hold Time	t_{KHQX}	0.5	-	0.5	-	0.5	-	ns	1
Clock High to Output High-z	t_{KHQZ}	-	2.5	-	3.0	-	3.5	ns	1, 2
Clock high to Output Active	t_{XHQX4}	1.0	-	1.0	-	1.0	-	ns	1, 2
Output Enable to High-z	t_{GHQZ}	-	2.5		3.0	-	3.5	ns	1, 2
Output Enable to Low-z	t_{GLQX}	0.5	-	0.5	-	0.5	-	ns	1, 2
Output Enable to Output Valid	t_{GLQV}	-	2.5	-	3.0	-	3.5	ns	1
Output Enable Setup Time	t_{GHKH}	0.5	-	0.5	-	0.5	-	ns	1, 3
Output Enable Hold Time	t_{KHGX}	1.5	-	1.5	-	1.5	-	ns	1, 3
Sleep Mode Recovery Time	t_{ZZR}	5	-	6	-	7	-	ns	
Sleep Mode Enable Time	t_{ZZE}	-	5	-	6	-	7	ns	

1.See AC Test Loading figure on page 8.
2.Transitions are measured ± 200mV from steady state voltage.
3.Output Driver Impedance update specifications for $\overline{G}$ induced updates. Write and Deselect cycles will also induce Output Driver Updates during High-z.
4.Inuse conditions V_{IH}, V_{IL}, Trise, Tfall of inputs must be withim 20% of V_{IH}, V_{IL}, Trise, Tfall of Clock.

Timing Diagram (Read and Deselect Cycles)

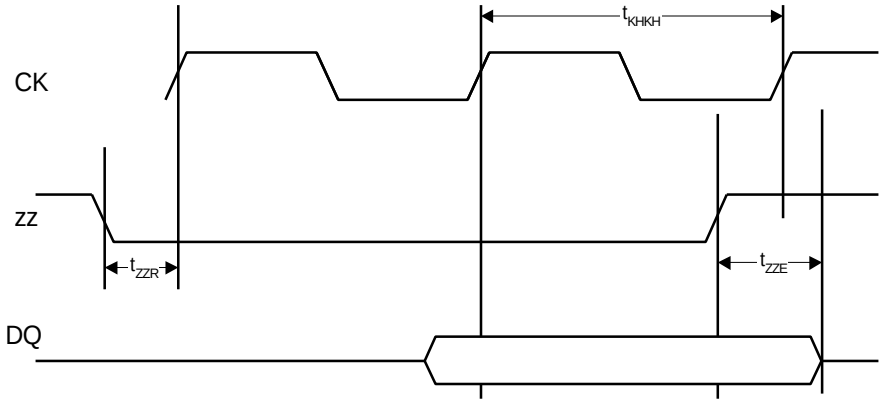


Timing Diagram (Read Write Cycles)



NOTES:
1.D2 is the input data write in memory location A2.
2.Q2 is output data read from the write buffer, as a result of address A2 being a match from the last write cycle address.

Timing Diagram (Sleep Mode)



IEEE 1149.1 TAP AND BOUNDARY SCAN

The SRAM provides a limited set of JTAG functions intended to test the interconnection between SRAM I/Os and printed circuit board traces or other components. There is no multiplexer in the path from I/O pins to the RAM core.

In conformance with IEEE std. 1149.1, the SRAM contains a TAP controller, Instruction register, Boundary Scan register, Bypass register and ID register.

The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required.

Signal List

- TCK : Test Clock
- TMS : Test Mode Select
- TDI : Test Data In
- TDO : Test Data Out

Caution: TCK, TMS, TDI must be tied down, even if JTAG is not used.

JTAG Recommended DC Operating Conditions (T_J = 0 to 110 °C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
JTAG Input High Voltage	V_{IH1}	2.2	-	V_{DD} + 0.3	V	1
JTAG Input Low Voltage	V_{IL1}	-03	-	0.8	V	1
JTAG Output High Level	V_{OH1}	2.4	-	-	V	1,2
JTAG Output Low Level	V_{OL1}	-	-	0.4	V	1,3

1. All JTAG Inputs/Outputs are LVTTL Compatible only.
2. I_{OH1} = -8mA at 2.4V.
3. I_{OL1} = +8mA at 0.4V.

JTAG Recommended DC Operating Conditions (T_J = 0 to 110 °C)

Parameter	Symbol	Conditions	Units	Notes
Input Pulse High Level	V_{IH1}	3.0	V	
Input Pulse Low Level	V_{IL1}	0.0	V	
Input Rise Time	T_{R1}	2.0	ns	
Input Fall Time	T_{F1}	2.0	ns	
Input and Output Timing Reference Level		1.5	V	1

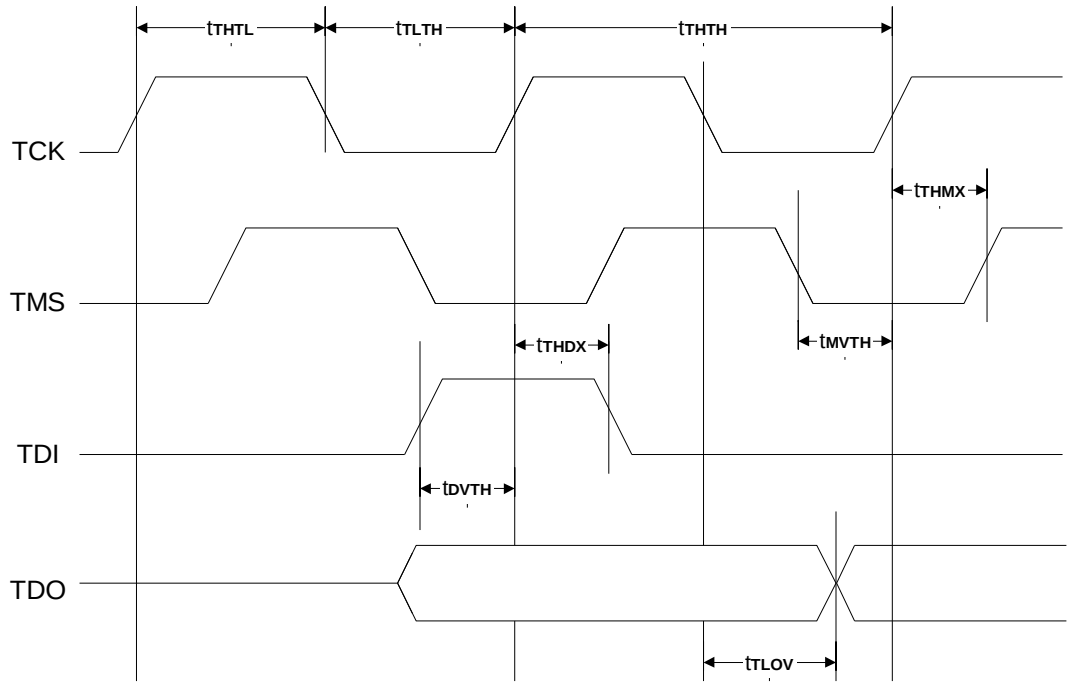
1. See AC Test Loading on page 8.

JTAG AC Characteristics (T_J = 0 to 110 °C, V_{DD} = 3.3V ± 5%)

Parameter	Symbol	Min.	Max.	Units	Notes
TCK Cycle Time	t_{THTH}	20	-	ns	
TCK High Pulse Width	t_{THTL}	7	-	ns	
TCK Low Pulse Width	t_{TLTH}	7	-	ns	
TMS Setup	t_{MVTH}	4	-	ns	
TMS Hold	t_{THMX}	4	-	ns	
TDI Setup	t_{DVTH}	4	-	ns	
TDI Hold	t_{THDX}	4	-	ns	
TCK Low to Valid Data	t_{TLOV}	-	7	ns	1

1. See AC Test Loading on page 8.

JTAG Timing Diagram



Scan Register Definition

Register Name	Bit Size X18	Bit Size X 36
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan*	51	70

* The Boundary Scan chain consists of the following bits :
  - 36 or 18 bits for Data Inputs Depending on X 18 or X 36 Configuration
  - 15 bits for SA0 - SA14 for X 36, 16 bits for SA0 - SA15 for X 18
  - 4 bits for $\overline{SBWa}$ - $\overline{SBWd}$ in X 36, 2 bits for $\overline{SBWa}$ and $\overline{SBWb}$ X 18
  - 9 bits for CK, $\overline{CK}$, ZQ, $\overline{SS}$, $\overline{G}$, $\overline{SW}$, ZZ, M1 and M2
  - 6 bits for Place Holders

* CK and $\overline{CK}$ clocks connect to a differential receiver that generates a single-ended clock signal. This signal and its inverted value are used for Boundary Scan sampling.

ID Register Definition

Part	Field Bit Number and Description				
	Revision Number (31 : 28)	Device Density and Configuration (27 : 18)	Vender Definition (17 : 12)	Manufacture JEDEC Code (11 : 1)	Start Bit (0)
256K X 18	0001	100 000 0110	000001	000 101 111 11	1
128K X 36	0001	011 100 1101	100001	000 101 111 11	1

Instruction Set

Code	Instruction	Notes
000	SAMPLE-Z	1
001	IDCODE	1
010	SAMPLE-Z	1
011	PRIVATE	3
100	SAMPLE	4
101	PRIVATE	3
110	PRIVATE	3
111	BYPASS	3

1. Places DQs in High-Z in order to sample all input data regardless of the other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. BYPASS register is initiated to Vss when BYPASS instruction is invoked. The BYPASS register also holds the last serially loaded TDI when exiting the Shift DR state.
4. SAMPLE instruction does not place DQs in High-Z

List of IEEE 1149.1 standard violations :

- 7.2.1.b,e
- 7.7.1.a-f
- 10.1.1.b,e
- 10.7.1.a-d
- 6.1.1.d

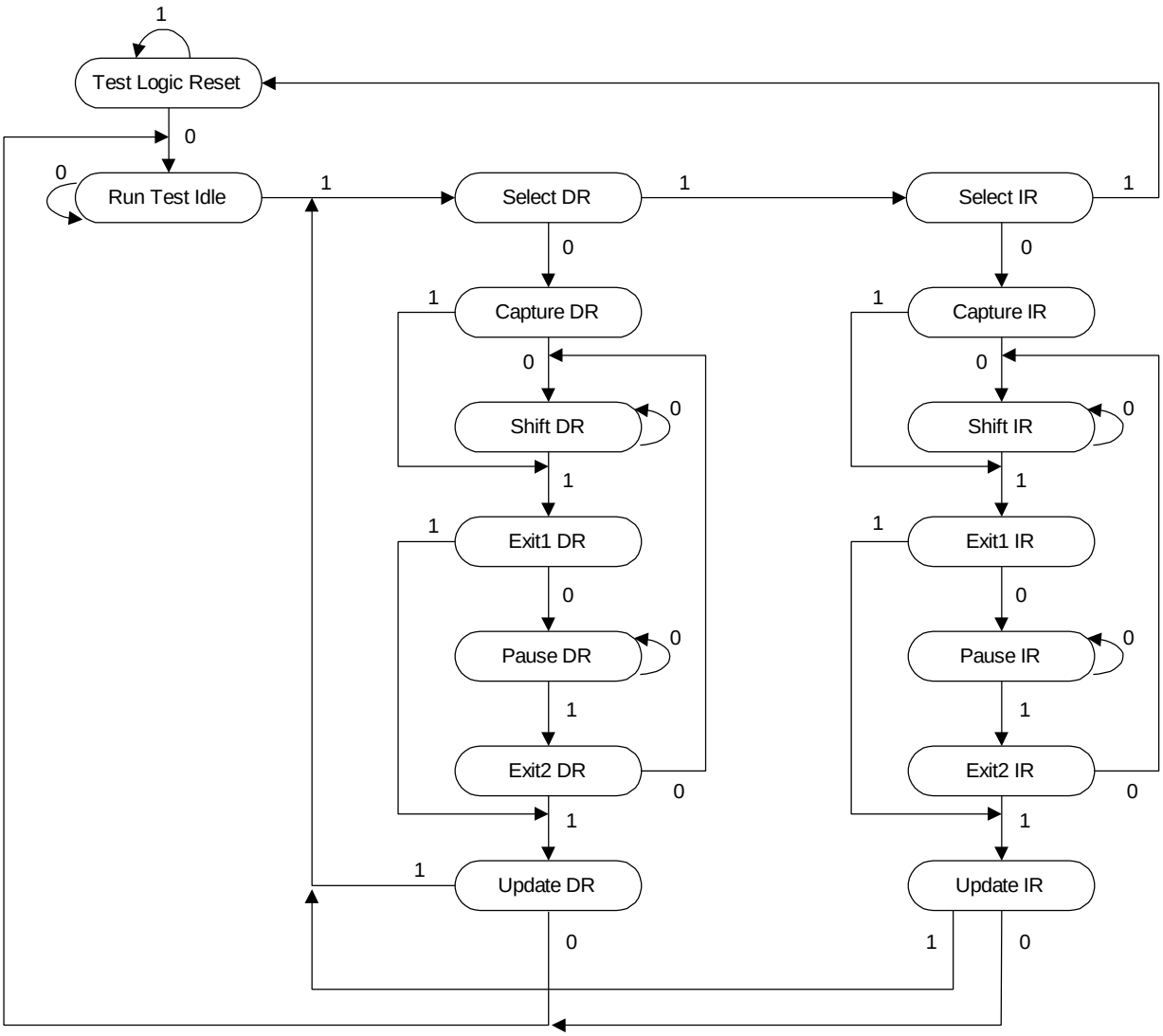
Boundary Scan Order (X 36)

Exit Order	Signal	Bump #	Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	M2	5R	25	DQ13	6F	49	DQ26	2H
2	SA1	4P	26	DQ11	7E	50	DQ25	1H
3	SA2	4T	27	DQ12	6E	51	$\overline{\text{SBWc}}$	3G
4	SA12	6R	28	DQ9	7D	52	ZQ	4D
5	SA13	5T	29	DQ10	6D	53	$\overline{\text{SS}}$	4E
6	ZZ	7T	30	SA14	6A	54	NC	4G
7	DQ1	6P	31	SA15	6C	55	NC	4H
8	DQ0	7P	32	SA10	5C	56	$\overline{\text{SW}}$	4M
9	DQ3	6N	33	SA16	5A	57	$\overline{\text{SBWd}}$	3L
10	DQ2	7N	34	NC	6B	58	DQ34	1K
11	DQ4	6M	35	SA11	5B	59	DQ35	2K
12	DQ6	6L	36	SA8	3B	60	DQ32	1L
13	DQ5	7L	37	NC	2B	61	DQ33	2L
14	DQ8	6K	38	SA7	3A	62	DQ31	2M
15	DQ7	7K	39	SA9	3C	63	DQ29	1N
16	$\overline{\text{SBWa}}$	5L	40	SA6	2C	64	DQ30	2N
17	$\overline{\text{CK}}$	4L	41	SA5	2A	65	DQ27	1P
18	CK	4K	42	DQ19	2D	66	DQ28	2P
19	$\overline{\text{G}}$	4F	43	DQ18	1D	67	SA3	3T
20	$\overline{\text{SBWb}}$	5G	44	DQ21	2E	68	SA4	2R
21	DQ16	7H	45	DQ20	1E	69	SA0	4N
22	DQ17	6H	46	DQ22	2F	70	M1	3R
23	DQ14	7G	47	DQ24	2G			
24	DQ15	6G	48	DQ23	1G			

Boundary Scan Order (X 18)

Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	M2	5R	27	NC	2B
2	SA12	6T	28	SA7	3A
3	SA1	4P	29	SA9	3C
4	SA13	6R	30	SA6	2C
5	SA17	5T	31	SA5	2A
6	ZZ	7T	32	DQ9	1D
7	DQ0	7P	33	DQ12	2E
8	DQ3	6N	43	DQ15	2G
9	DQ6	6L	35	DQ16	1H
10	DQ7	7K	36	$\overline{SBWb}$	3G
11	$\overline{SBWa}$	5L	37	ZQ	4D
12	$\overline{CK}$	4L	38	$\overline{SS}$	4E
13	CK	4K	39	NC	4G
14	$\overline{G}$	4F	40	NC	4H
15	DQ8	6H	41	$\overline{SW}$	4M
16	DQ5	7G	42	DQ17	2K
17	DQ4	6F	43	DQ14	1L
18	DQ2	7E	44	DQ13	2M
19	DQ1	6D	45	DQ11	1N
20	SA14	6A	46	DQ10	2P
21	SA15	6C	47	SA3	3T
22	SA10	5C	48	SA4	2R
23	SA16	5A	49	SA0	4N
24	NC	6B	50	SA2	2T
25	SA11	5B	51	M1	3R
26	SA8	3B			

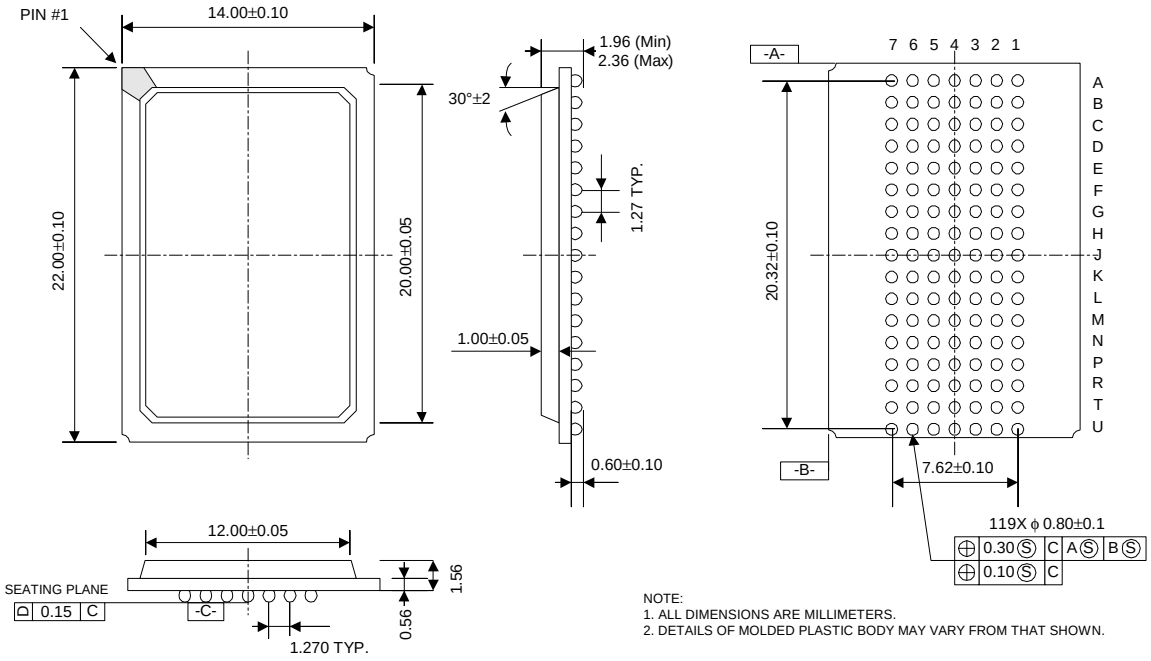
TAP Controller State Machine



Ordering Information

Part Number	Organization	Speed	Package
A65H83181P-5	256K x 18	2.5ns Access / 5 ns Cycle	7 x 17 PBGA
A65H83181P-6	256K x 18	3.0ns Access / 6 ns Cycle	7 x 17 PBGA
A65H83181P-7	256K x 18	3.5ns Access / 7 ns Cycle	7 x 17 PBGA
A65H73361P-5	128K x 36	2.5ns Access / 5 ns Cycle	7 x 17 PBGA
A65H73361P-6	128K x 36	3.0ns Access / 6 ns Cycle	7 x 17 PBGA
A65H73361P-7	128K x 36	3.5ns Access / 7 ns Cycle	7 x 17 PBGA

Package Information



NOTE:
1. ALL DIMENSIONS ARE MILLIMETERS.
2. DETAILS OF MOLDED PLASTIC BODY MAY VARY FROM THAT SHOWN.