Device Features

- Fully qualified Bluetooth system
- Low power 1.8V operation
- Minimum external components
- Integrated 1.8V regulator
- UART Bypass mode
- Available in VFBGA and CSP packages
- Available in 'RF Plug and Go' package (see separate data sheet)

BlueCore™2-ROM

Single Chip Bluetooth® System

Production Information Data Sheet for

BC213143A

June 2003

General Description

BlueCore2-ROM is a single chip radio and baseband chip for Bluetooth wireless technology 2.4GHz systems.
It is implemented in 0.18µm CMOS technology.

BlueCore2-ROM has the same pinout and electrical characteristics as available in BlueCore2-Flash to enable development of custom code before committing to ROM.

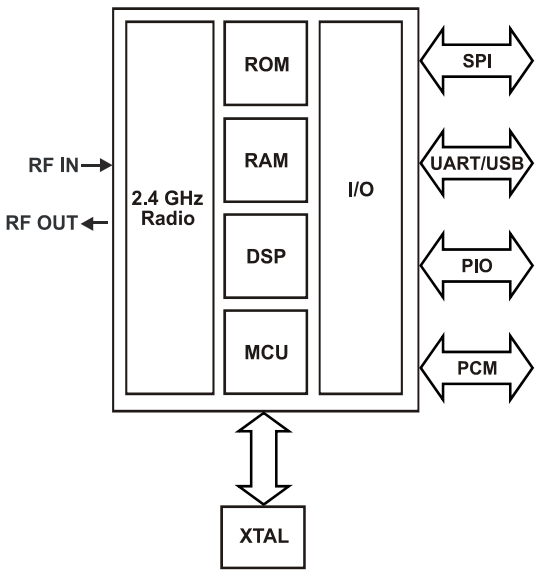
The 4Mbit ROM is metal programmable, which enables a six week turn-around from approval of firmware to production samples.

Applications

- Cellular Handsets
- Personal Digital Assistants
- Mice
- Keyboards
- High volume, cost sensitive production

BlueCore2-ROM has been designed to reduce the number of external components required which ensures production costs are minimised.

The device incorporates auto-calibration and built-in-self-test (BIST) routines to simplify development, type approval and production test. All hardware and device firmware is fully compliant with the Bluetooth specification v1.1.



System Architecture

Production Information

Contents

1 Key Features 5
2 6 x 6 VFBGA Package Information 6
2.1 BC213143AXX-EK and BC213143AXX-RK Pinout Diagram 6
2.2 Device Terminal Functions 7
3 4 x 4 CSP Package Information 10
3.1 BC213143AXX-XB Pinout Diagram 10
3.2 Device Terminal Functions 11
4 Electrical Characteristics 14
5 Radio Characteristics 19
5.1 Temperature +20°C 19
5.1.1 Transmitter 19
5.1.2 Receiver 20
5.1.3 Blocking 21
5.2 Temperature -40°C 22
5.2.1 Transmitter 22
5.2.2 Receiver 22
5.3 Temperature -25°C 23
5.3.1 Transmitter 23
5.3.2 Receiver 23
5.4 Temperature +85°C 24
5.4.1 Transmitter 24
5.4.2 Receiver 24
5.5 Temperature +105°C 25
5.5.1 Transmitter 25
5.5.2 Receiver 25
5.6 Power Consumption 26
6 Device Diagrams 27
7 Description of Functional Blocks 28
7.1 RF Receiver 28
7.1.1 Low Noise Amplifier 28
7.1.2 Analogue to Digital Converter 28
7.2 RF Transmitter 28
7.2.1 IQ Modulator 28
7.2.2 Power Amplifier 28
7.2.3 Auxiliary DAC 28
7.3 RF Synthesiser 28
7.4 Clock Input and Generation 28
7.5 Baseband and Logic 29
7.5.1 Memory Management Unit 29
7.5.2 Burst Mode Controller 29
7.5.3 Physical Layer Hardware Engine DSP 29
7.5.4 RAM 29
7.5.5 ROM 29
7.5.6 USB 29
7.5.7 Synchronous Serial Interface 29
7.5.8 UART 29
7.5.9 Audio PCM Interface 29
7.6 Microcontroller 30
7.6.1 Programmable I/O 30
8 CSR Bluetooth Software Stacks 31
8.1 Important Information 31
8.2 BlueCore HCI Stack 31
8.2.1 Key Features of the HCI Stack 32
8.3 BlueCore RFCOMM Stack 34
8.3.1 Key Features of the BlueCore2-ROM RFCOMM Stack 34

8.4 BlueCore Virtual Machine Stack 35
8.5 BlueCore HID Stack 36
8.6 Host Side Software 37
8.7 Additional Software for Other Embedded Applications 37
8.8 CSR Development Systems 37
9 Application Schematics 38
9.1 6 x 6 VFBGA 84-Ball Package 38
9.1.1 Application Schematic using Separate Balun and Filter 38
9.1.2 Application Schematic using Epcos Combined Balun and Filter 39
9.1.3 Application Schematic using Soshin Combined Balun and Filter 40
9.2 4 x 4 CSP 49-Ball Package 41
10 Package Dimensions 42
10.1 6 x 6 VFBGA 84-Ball Package 42
10.2 4 x 4 CSP 47-Ball Package 43
11 Ordering Information 44
11.1 BlueCore2-ROM 44
12 Contact Information 45
13 Document References 46
Acronyms and Definitions 47
Status Information 49
Record of Changes 50

List of Figures

Figure 6.1: BlueCore2-ROM Device Diagram for 6 x 6mm VFBGA and 4 x 4mm CSP Packages 27
Figure 8.1: BlueCore HCI Stack 31
Figure 8.2: BlueCore RFCOMM Stack 34
Figure 8.3: Virtual Machine 35
Figure 8.4: HID Stack 36
Figure 9.1: Application Circuit using Separate Balun and Filter for 6 x 6 VFBGA Package 38
Figure 9.2: Application Circuit using Epcos Balun and Filter for 6 x 6 VFBGA Package 39
Figure 9.3: Application Circuit using Soshin Balun and Filter for 6 x 6 VFBGA Package 40
Figure 9.4: Application Circuit for 4 x 4 CSP Package 41
Figure 10.1: BlueCore2-ROM VFBGA Package Dimensions 42
Figure 10.2: BlueCore2-ROM CSP Package Dimensions 43

1 Key Features

Radio

- Operation with common TX/RX terminals simplifies external matching circuitry and eliminates external antenna switch
- Extensive built-in-self-test minimises production test time
- No external trimming is required in production
- Full RF reference designs are available

Transmitter

- Up to +6dBm RF transmit power with level control from the on-chip 6-bit DAC over a dynamic range greater than 30dB
- Supports Class 2 and Class 3 radios without the need for an external power amplifier or TX/RX switch
- Supports Class 1 radios with an external power amplifier, provided by a power control terminal controlled by an internal 8-bit voltage DAC and an external RF TX/RX switch

Receiver

- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Digitised RSSI available in real time over the HCI interface
- Fast AGC for enhanced dynamic range

Synthesiser

- Fully integrated synthesizer; no external VCO varactor diode, resonator or loop filter
- Compatible with crystals between 8 and 32MHz (in multiples of 250kHz) or an external clock
- Accepts 7.68, 14.4, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz TCXO frequencies for GSM and CDMA devices with either sinusoidal or logic level signals

Auxiliary Features

- Crystal oscillator with built-in digital trimming
- Power management includes digital shut down and wake up commands and an integrated low power oscillator for ultra low Park/Sniff/Hold mode power consumption
- Device can be used with an external master oscillator and provides a ‘clock request signal’ to control external clock source

Auxiliary Features

- On-chip linear regulator, producing 1.8V output from 2.2 – 4.2V input
- Power on reset cell detects low supply voltage
- Arbitrary sequencing of power supplies is permitted
- Uncommitted 8-bit ADC and 8-bit DAC are available to application programs

Baseband and Software

- Internal programmed 4Mbit ROM for complete system solution
- 32Kbyte on-chip RAM allows full speed Bluetooth data transfer, mixed voice and data, plus full seven Slave piconet operation
- Dedicated logic for forward error correction, header error control, access code correlation, demodulation, cyclic redundancy check, encryption bitstream generation, whitening and transmit pulse shaping
- Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air

Physical Interfaces

- Synchronous serial interface up to 4M Baud for system debugging
- UART interface with programmable Baud rate up to 1.5M Baud with an optional bypass mode
- Full speed USB interface supports OHCI and UHCI host interfaces. Compliant with USB v2.0
- Synchronous bi-directional serial programmable audio interface
- Optional I^2C™ compatible interface

Bluetooth Stack

CSR’s Bluetooth Protocol Stack runs on-chip in a variety of configurations:

- Standard HCI (UART or USB)
- Fully embedded to RFCOMM
- Customer specific builds with embedded application code

Package Options

- 84-ball VFBGA 6 x 6 x 1.0mm 0.5mm pitch
- 49-ball CSP 4 x 4 x 0.7mm 0.5mm pitch

2 6 x 6 VFBGA Package Information

2.1 BC213143AXX-EK and BC213143AXX-RK Pinout Diagram

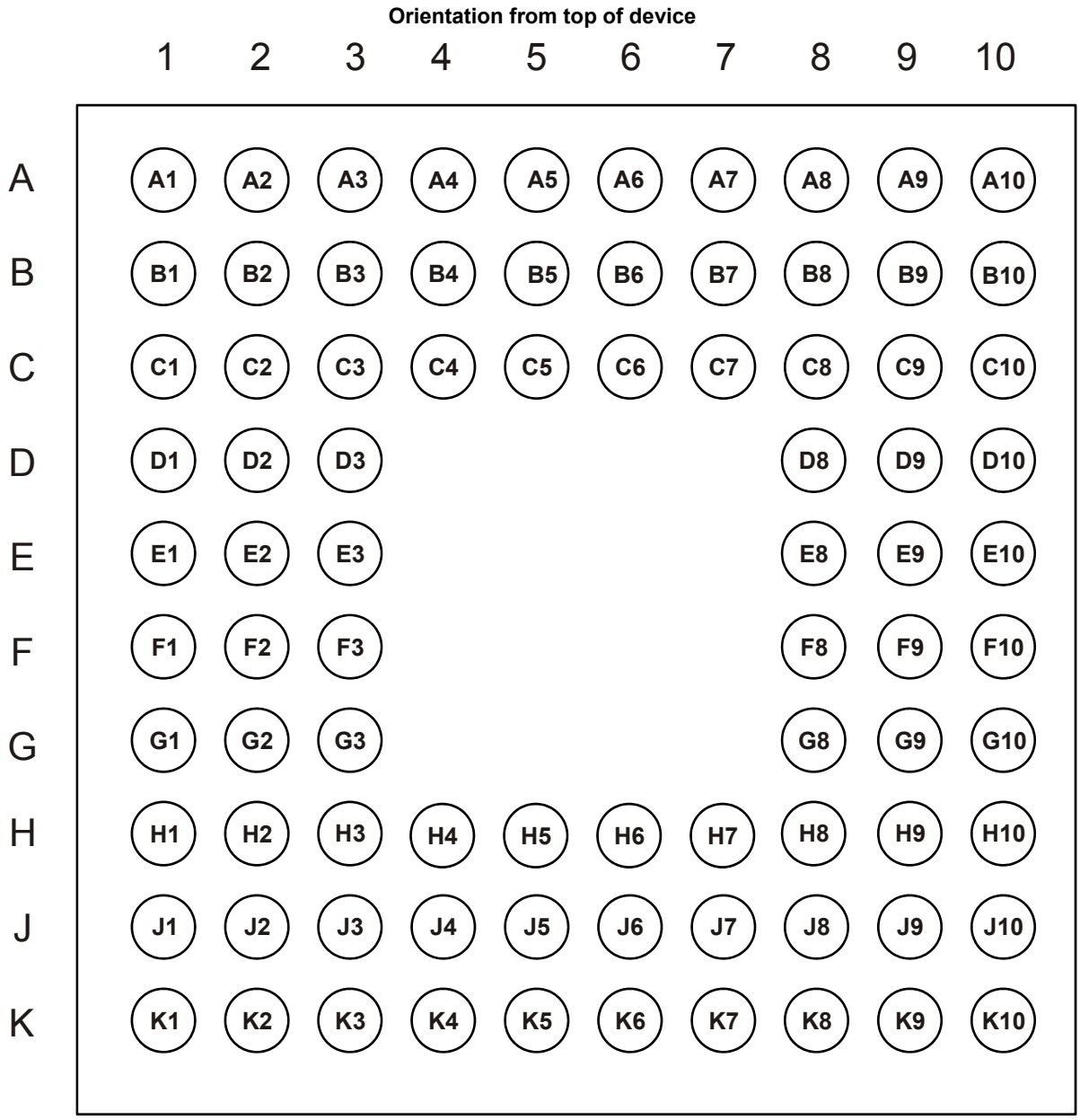


Figure 2.1: BlueCore2-ROM 6 x 6mm Packages (BC213143AXX-EK and BC213143AXX-RK)

2.2 Device Terminal Functions

Radio	Ball	Pad Type	Description
RF_IN	D1	Analogue	Single ended receiver input
PIO[0]/RXEN	B1	Bi-directional with programmable strength internal pull-up/down	Control output for external LNA (if fitted)
PIO[1]/TXEN	B2	Bi-directional with programmable strength internal pull-up/down	Control output for external PA (if fitted for Class 1)
TX_A	F1	Analogue	Transmitter output/switched receiver input
TX_B	E1	Analogue	Complement of TX_A
AUX_DAC	D3	Analogue	Voltage DAC output

Synthesiser and Oscillator	Ball	Pad Type	Description
XTAL_IN	K3	Analogue	For crystal or external clock input
XTAL_OUT	J3	Analogue	Drive for crystal
LOOP_FILTER	H2	Analogue	Connection to external PLL loop filter (Do not connect)

PCM Interface	Ball	Pad Type	Description
PCM_OUT	G8	CMOS output, tristatable with weak internal pull-down	Synchronous data output
PCM_IN	G9	CMOS input, with weak internal pull-down	Synchronous data input
PCM_SYNC	G10	Bi-directional with weak internal pull-down	Synchronous data sync
PCM_CLK	H10	Bi-directional with weak internal pull-down	Synchronous data clock

USB and UART	Ball	Pad Type	Description
UART_TX	J10	CMOS output, tristatable with weak internal pull-up	UART data output active low
UART_RX	H9	CMOS input with weak internal pull-down	UART data input active low (idle status high)
UART_RTS	H7	CMOS output, tristatable with weak internal pull-up	UART request to send active low
UART_CTS	H8	CMOS input with weak internal pull-down	UART clear to send active low
USB_DP	J8	Bi-directional	USB data plus with selectable internal 1.5kΩ pull-up resistor
USB_DN	K8	Bi-directional	USB data minus

Test and Debug	Ball	Pad Type	Description
RESET	C7	CMOS input with weak internal pull-down	Reset if high. Input debounced so must be high for >5ms to cause a reset
RESET_B	D8	CMOS input with weak internal pull-up	Reset if low. Input debounced so must be low for >5ms to cause a reset
SPI_CSB	C9	CMOS input with weak internal pull-up	Chip select for Serial Peripheral Interface, active low
SPI_CLK	C10	CMOS input with weak internal pull-down	Serial Peripheral Interface clock
SPI_MOSI	C8	CMOS input with weak internal pull-down	Serial Peripheral Interface data input
SPI_MISO	B9	CMOS output, tristatable with weak internal pull-down	Serial Peripheral Interface data output
TEST_EN	C6	CMOS input with strong internal pull-down	For test purposes only (leave unconnected)
FLASH_EN	B8	No pad	Pull high to VDD_MEM for compatibility with flash parts

PIO Port	Ball	Pad Type	Description
PIO[2]	B3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[3]	B4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[4]	E8	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[5]	F8	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[6]	F10	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[7]	F9	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[8]	C5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[9]	C3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[10]	C4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[11]	E3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
AIO[0]	H4	Bi-directional	Programmable input/output line
AIO[1]	H5	Bi-directional	Programmable input/output line
AIO[2]	J5	Bi-directional	Programmable input/output line

Power Supplies and Control	Ball	Pad Type	Description
VREG_IN	K6	Regulator input	Linear regulator voltage input
VDD_USB	K9	VDD	Positive supply for UART/USB ports
VDD_PIO	A3	VDD	Positive supply for PIO and AUX DAC(1)
VDD_PADS	D10	VDD	Positive supply for all other digital input/output ports(2)
VDD_MEM	A6,A7, A9, H6, J6, K7	VDD	Positive supply AIO ports (and flash memory on flash parts)
VDD_CORE	E10	VDD	Positive supply for internal digital circuitry and internal ROM
VDD_RADIO	C1, C2	VDD	Positive supply for RF circuitry
VDD_VCO	H1	VDD	Positive supply for VCO and synthesiser circuitry
VDD_ANA	K4	VDD/Regulator output	Positive supply for analogue circuitry and 1.8V regulated output
VSS_PADS	A1, A2, D9, J9, K10	VSS	Ground connection for input/output
VSS_MEM	A10, B5, B7, B10, J7	VSS	Ground connections AIO ports (and flash memory on flash parts)
VSS_CORE	E9	VSS	Ground connection for internal digital circuitry and internal ROM
VSS_RADIO	D2, E2, F2	VSS	Ground connections for RF circuitry
VSS_VCO	G1, G2	VSS	Ground connections for VCO and synthesiser
VSS_ANA	J2, J4, K2	VSS	Ground connections for analogue circuitry
VSS	F3	VSS	Ground connection for internal package shield

Unconnected Terminals	Ball	Description
	A4, A5, A8, B6, G3, H3, J1, K1, K5	Leave unconnected

Notes:

(1) Positive supply for PIO[3:0] and PIO[11:8]

(2) Positive supply for SPI/PCM ports and PIO[7:4]

See Section 4, Electrical Characteristics, for voltage specifications

3 4 x 4 CSP Package Information

3.1 BC213143AXX-XB Pinout Diagram

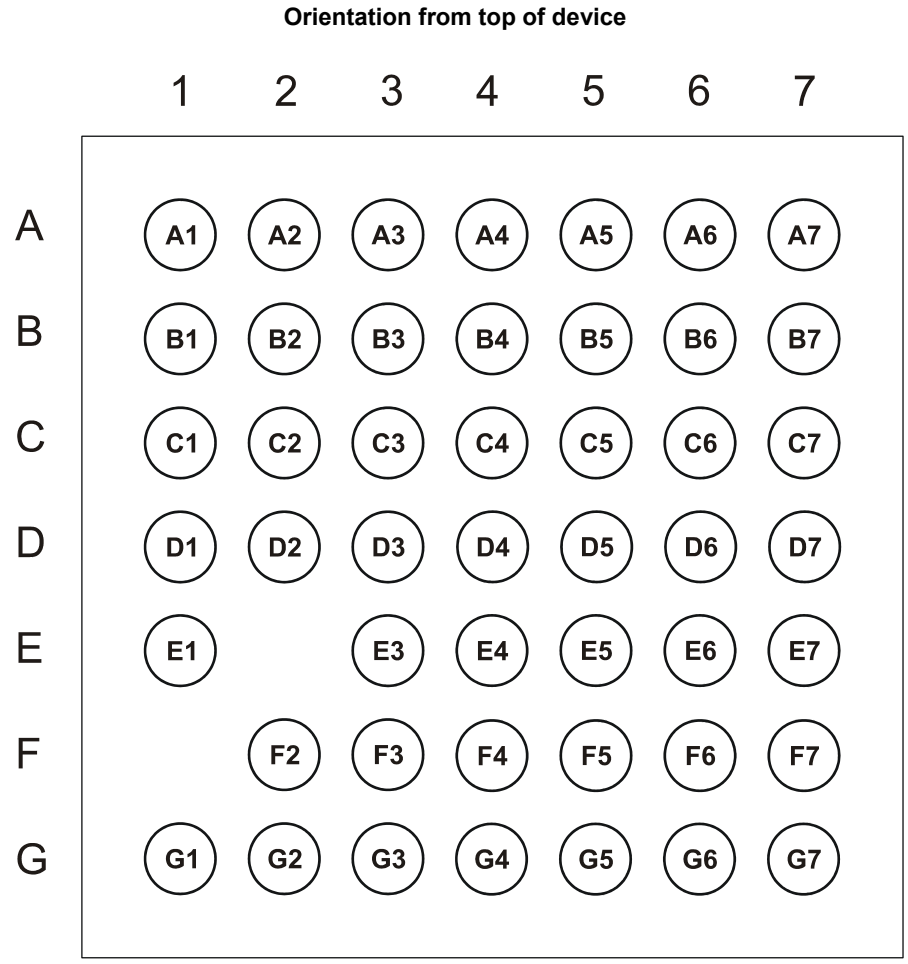


Figure 3.1: BlueCore2-ROM 4 x 4mm CSP Package (BC213143AXX-XB)

Note:

Performance and characterisation data reported is not guaranteed for the CSP package option. All data should be regarded as Pre-Production Information with respect to the CSP package.

3.2 Device Terminal Functions

Radio	Ball	Pad Type	Description
PIO[0]/RXEN	G3	Bi-directional with programmable strength internal pull-up/down	Control output for external LNA (if fitted) (=PIO[0])
PIO[1]/TXEN	E3	Bi-directional with programmable strength internal pull-up/down	Control output for external PA Class 1 only (=PIO[1])
TX_A	G2	Analogue	Transmitter output/Switched Receiver input
TX_B	G1	Analogue	Complement of TX_A
AUX_DAC	F2	Analogue	Voltage DAC output

Synthesiser and Oscillator	Ball	Pad Type	Description
XTAL_IN	A1	Analogue	For crystal or external clock input
XTAL_OUT	A2	Analogue	Drive for crystal

PCM Interface	Ball	Pad Type	Description
PCM_OUT	C7	CMOS output, tristatable with weak internal pull-down	Synchronous data output
PCM_IN	C5	CMOS input, with weak internal pull-down	Synchronous data input
PCM_SYNC	C6	Bi-directional with weak internal pull-down	Synchronous data sync
PCM_CLK	D5	Bi-directional with weak internal pull-down	Synchronous data clock

USB and UART	Ball	Pad Type	Description
UART_TX	B7	CMOS output, tristatable with weak internal pull-up	UART data output active low
UART_RX	B6	CMOS input with weak internal pull-down	UART data input active low (idle status high)
UART_RTS	B5	CMOS output, tristatable with weak internal pull-up	UART request to send active low
UART_CTS	C4	CMOS input with weak internal pull-down	UART clear to send active low
USB_DP	A5	Bi-directional	USB data plus with selectable internal 1.5kΩ pull-up resistor
USB_DN	A6	Bi-directional	USB data minus

Test and Debug	Ball	Pad Type	Description
RESETB	E4	CMOS input with weak internal pull-up	Reset if low. Input debounced so must be low for >5ms to cause a reset
SPI_CSB	G6	CMOS input with weak internal pull-up	Chip select for Synchronous Serial Interface active low
SPI_CLK	F5	CMOS input with weak internal pull-down	Serial Peripheral Interface clock
SPI_MOSI	F7	CMOS input with weak internal pull-down	Serial Peripheral Interface data input
SPI_MISO	G7	CMOS output, tristatable with weak internal pull-down	Serial Peripheral Interface data output
TEST_EN	D2	CMOS input with strong internal pull-down	For test purposes only (leave unconnected)

PIO Port	Ball	Pad Type	Description
PIO[2]	D3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[3]	F4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[4]	E5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[5]	D7	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[6]	D6	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[7]	D4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[8]	F3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
AIO[0]	B3	Bi-directional	Programmable input/output line
AIO[1]	C2	Bi-directional	Programmable input/output line
AIO[2]	C3	Bi-directional	Programmable input/output line

Power Supplies and Control	Ball	Pad Type	Description
VREG_IN	A4	Regulator input	Linear regulator voltage input
VDD_USB	B4	VDD	Positive supply for UART/USB and AIO ports
VDD_PIO	G5	VDD	Positive supply for PIO and AUX DAC(1)
VDD_PADS	F6	VDD	Positive supply for all other digital input/output ports (2)
VDD_CORE	E6	VDD	Positive supply for internal digital circuitry
VDD_RADIO	D1	VDD	Positive supply for RF circuitry
VDD_VCO	B1	VDD/ Regulator input	Positive supply for VCO and synthesiser circuitry
VDD_ANA	A3	VDD	Positive supply for analogue circuitry and 1.8V regulated output
VSS_PADS	A7, E7, G4	VSS	Ground connection for internal digital circuitry and input/output
VSS_RADIO	E1	VSS	Ground connections for RF circuitry
VSS_VCO	C1	VSS	Ground connections for VCO and synthesiser
VSS_ANA	B2	VSS	Ground connections for analogue circuitry

Notes:

(1) Positive supply for PIO[3:0] and PIO[8].

(2) Positive supply for SPI/PCM ports and PIO[7:4].

4 Electrical Characteristics

Absolute Maximum Ratings		
Rating	**Min**	**Max**
Storage Temperature	-40°C	150°C
Supply Voltage: VDD_RADIO, VDD_VCO, VDD_ANA, VDD_CORE and VDD_MEM	-0.4V	2.2V
Supply Voltage: VDD_PADS, VDD_PIO, VDD_USB	-0.4V	3.7V
Supply Voltage: VREG_IN	-0.4V	4.2V
Other Terminal Voltages	VSS-0.4V	VDD+0.4V

Recommended Operating Conditions		
Operating Condition	**Min**	**Max**
Guaranteed RF performance range	-40°C	105°C
Supply Voltage: VDD_RADIO, VDD_VCO, VDD_ANA, VDD_CORE and VDD_MEM	1.7V	1.9V
Supply Voltage: VDD_PADS, VDD_PIO, VDD_USB	1.7V	3.6V
Supply Voltage: VREG_IN(1)	2.2V	3.6V(2)

Note:

(1) If the internal linear regulator is not required VREG_IN should be connected to 1.8V.

(2) The device will operate with VREG_IN as high as 4.2V, however performance is not guaranteed above 3.6V.

Input/Output Terminal Characteristics[1]				
Linear Regulator	**Min**	**Typ**	**Max**	**Unit**
Normal Operation				
Output Voltage (Iload = 70mA / VREG_IN = 3.0V)	1.70	1.78	1.85	V
Temperature Coefficient	-250	-	250	ppm/C
Output Noise[2][3]	-	-	1	mV rms
Load Regulation (Iload < 100mA)[8]	-	-	50	mV/A
Settling Time[2][4]	-	-	50	µs
Line Regulation[2][5]	-20	-	-	dB
Maximum Output Current	100	-	-	mA
Minimum Load Current	5	-	-	µA
Dropout Voltage (Iload = 70mA)	-	-	350	mV
Quiescent Current (excluding load, Iload <1mA)	25	35	50	µA
Low Power Mode[6]				
Quiescent Current (excluding load, Iload <100µA)	4	7	10	µA
Disabled Mode[7]				
Quiescent Current	1.5	2.5	3.5	µA

Notes:

(1) These parameters are guaranteed for 2.2 to 3.6V. Between 3.6V and 4.2V the output voltage is not guaranteed to remain below 1.85V, but full functionality of the chip will be preserved and no damage will ensue.

(2) Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors

(3) Frequency range 100Hz to 100kHz

(4) 1mA to 70mA pulsed load

(5) Frequency range 100Hz to 10MHz

(6) Low power mode is entered and exited automatically when the chip enters/leaves Deep Sleep mode

(7) Regulator is disabled when VREG_IN is either open circuit or driven to the same voltage as VDD_ANA

(8) On-chip voltage: This figure does not include bondwire or ball-to-PCB resistance effects.

Input/Output Terminal Characteristics (Continued)					
Digital Terminals		**Min**	**Typ**	**Max**	**Unit**
Input Voltage Levels					
V_{IL} input logic level low	2.7 ≤VDD ≤3.6	-0.4	-	0.8	V
	1.7 ≤VDD ≤1.9	-0.4	-	0.4	V
V_{IH} input logic level high		0.7VDD	-	VDD+0.4	V
Output Voltage Levels					
V_{OL} output logic level low, (I_O = 4.0mA)	2.7 ≤VDD ≤3.6	-	-	0.2	V
V_{OL} output logic level low, (I_O = 4.0mA)	1.7 ≤VDD ≤1.9	-	-	0.4	V
V_{OH} output logic level high, (I_O = -4.0mA)	2.7 ≤VDD ≤3.6	VDD-0.2	-	-	V
V_{OH} output logic level high, (I_O = -4.0mA)	1.7 ≤VDD ≤1.9	VDD-0.4	-	-	V
Input and Tristate Current with:					
Strong pull-up		-100	-40	-10	µA
Strong pull-down		10	40	100	µA
Weak pull-up		-5	-1	0	µA
Weak pull-down		0	1	5	µA
I/O pad leakage current		-1	0	1	µA
CI Input Capacitance		1.0	-	5.0	pF

USB Terminals(1)	**Min**	**Typ**	**Max**	**Unit**
Input Threshold				
V_{IL} input logic level low	-	-	0.3 VDD_USB	V
V_{IH} input logic level high	0.57 VDD_USB	-	-	V
Input Leakage Current				
VSS_USB <V_{IN}< VDD_USB(2)	-1	1	5	µA
CI Input capacitance	2.5	-	10.0	pF
Output Voltage Levels To Correctly Terminated USB Cable				
V_{OL} output logic level low	0.0	-	0.2	V
V_{OH} output logic level high	2.8	-	VDD_USB	V

Input/Output Terminal Characteristics (Continued)				
Auxiliary DAC, 8-Bit Resolution	**Min**	**Typ**	**Max**	**Unit**
Resolution	-	-	8	Bits
Average output step size(3)	12.5	14.5	17.0	mV
Output Voltage		Monotonic(3)		
Voltage range (I_O=0mA)	VSS_PIO	-	VDD_PIO	V
Current range	-10.0	-	+0.1	mA
Minimum output voltage (I_O=100µA)	0.0	-	0.2	V
Maximum output voltage (I_O=10mA)	VDD_PIO-0.3	-	VDD_PIO	V
High Impedance leakage current	-1	-	1	µA
Offset	-220	-	120	mV
Integral non linearity(3)	-2	-	2	LSB
Starting time (50pF load)	-	-	10	µs
Settling time (50pF load)	-	-	5	µs

Crystal Oscillator	**Min**	**Typ**	**Max**	**Unit**
Crystal frequency(4) (7)	8.0	-	32.0	MHz
Digital trim range(5)	5.0	6.2	8.0	pF
Trim step size	-	0.1	-	pF
Transconductance	2.0	-	-	mS
Negative resistance(6)	870	1500	2400	Ω
External Clock				
Input frequency(7)	7.5	-	40.0	MHz
Clock input level(8)	0.4	-	VDD_ANA	V pk-pk
Phase noise (at zero crossing)	-	-	15	ps rms
XTAL_IN input impedance	10	-	-	kΩ
XTAL_IN input capacitance	-	7	10	pF
Power-on Reset				
VDD_CORE falling threshold	1.40	1.50	1.60	V
VDD_CORE rising threshold	1.50	1.60	1.70	V
Hysteresis	0.05	0.10	0.15	V

Notes:

VDD_CORE, VDD_RADIO, VDD_VCO, VDD_ANA and VDD_MEM are at 1.8V unless shown otherwise.

VDD_PADS, VDD_PIO and VDD_USB are at 3.0V unless shown otherwise

The same setting of the digital trim is applied to both XTAL_IN and XTAL_OUT.

Current drawn into a pin is defined as positive, current supplied out of a pin is defined as negative.

(1) 3.1V ≤VDD_USB ≤3.6V

(2) Internal USB pull-up disabled

(3) Specified for an output voltage between 0.2V and VDD_PIO -0.3V

(4) Integer multiple of 250kHz

(5) The difference between the internal capacitance at minimum and maximum settings of the internal digital trim

(6) XTAL frequency = 16MHz (Please refer to your software build release note for frequencies supported); XTAL C0 = 0.75pF; XTAL load capacitance = 8.5pF

(7) Clock input can be any frequency between 8 and 40MHz in steps of 250kHz + CDMA/3G TCXO frequencies of 7.68, 14.4, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz

(8) Clock input can either be sinusoidal or square wave. If the peaks of the signal are below VSS_ANA or above VDD_ANA a DC blocking capacitor is required between the signal and XTAL_IN

5 Radio Characteristics[5]

BlueCore2-ROM meets the Bluetooth specification v1.1 when used in a suitable application circuit between -40°C and +105°C.

5.1 Temperature +20°C

5.1.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +20°C					
	Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power[1]	3	6.5	-	-6 to +4[2]	dBm
RF power control range	25	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	820	1000	≤1000	kHz
Adjacent channel transmit power $F=F_0 \pm 2MHz$[3] [4]	-	-35	-20	≤-20	dBm
Adjacent channel transmit power $F=F_0 \pm 3MHz$[3] [4]	-	-45	-40	≤-40	dBm
Δf1avg “Maximum Modulation”	140	165	175	$140<\Delta f1_{avg}<175$	kHz
Δf2max “Minimum Modulation”	115	140	-	115	kHz
Δf2avg / Δf2avg	0.8	0.9	-	≥0.80	-
Initial carrier frequency tolerance	-	10	35	±75	kHz
Drift Rate	-	8	20	≤25	kHz/50µs
Drift (single slot packet)	-	9	20	≤25	kHz
Drift (five slot packet)	-	10	25	≤40	kHz

Notes:

(1) BlueCore2-ROM firmware maintains the transmit power to be within the Bluetooth specification v1.1 limits

(2) Class 2 RF transmit power range, Bluetooth specification v1.1

(3) Measured at F_0 = 2441MHz

(4) Up to three exceptions are allowed in v1.1 of the Bluetooth specification

(5) Performance and characterisation data reported is not guaranteed for the CSP package option. All data should be regarded as Pre-Production Information with respect to the CSP package.

5.1.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = +20°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER	2.402	-	-84	-80	≤-70	dBm
	2.441	-	-85	-81		
	2.480	-	-85	-81		
Maximum received signal at 0.1% BER		0	3	-	≥-20	
C/I co-channel		-	9	11	≤11	dB
Adjacent channel selectivity C/I $F=F_0+1MHz$ (1) (2)		-	-4	0	≤0	dB
Adjacent channel selectivity C/I $F=F_0-1MHz$ (1) (2)		-	-4	0	≤0	dB
Adjacent channel selectivity C/I $F=F_0+2MHz$ (1) (2)		-	-35	-30	≤-30	dB
Adjacent channel selectivity C/I $F=F_0-2MHz$ (1) (2)		-	-21	-20	≤-20	dB
Adjacent channel selectivity C/I $F\geq F_0+3MHz$ (1) (2)		-	-45	-	≤-40	dB
Adjacent channel selectivity C/I $F\leq F_0-5MHz$ (1) (2)		-	-45	-	≤-40	dB
Adjacent channel selectivity C/I $F=F_{Image}$ (1) (2)		-	-18	-9	≤-9	dB

Notes:

(1) Up to five exceptions are allowed in v1.1 of the Bluetooth specification

(2) Measured at F_0 = 2441MHz

5.1.3 Blocking

Radio Characteristics VDD = 1.8V Temperature = +20°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Emitted power in cellular bands measured at chip terminals Output power ≤4dBm	0.925 – 0.960[1]	-	-143	-138	-	dBmHz
	1.570 – 1.580[2]	-	-138	-135		
	1.805 – 1.880[1]	-	-131	-115		
	1.930 – 1.990[3]	-	-135	-125		
	1.930 – 1.990[1]	-	-135	-126		
	1.930 – 1.990[4]	-	-137	-130		
	2.110 – 2.170[4]	-	-132	-122		
	2.110 – 2.170[5]	-	-135	-127		
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Modulation**	**Unit**
Continuous power in cellular bands required to block Bluetooth reception[6] Measured at chip terminals	0.880 – 0.915	5	7	-	GSM	dBm
	1.710 – 1.785	3	6	-	GSM	
	1.850 – 1.910	1	5	-	GSM	
	1.920 – 1.980	-8	-6	-	W-CDMA	

Notes:

(1) Integrated in 200kHz bandwidth
(2) Integrated in 1MHz bandwidth
(3) Integrated in 30kHz bandwidth
(4) Integrated in 1.2MHz bandwidth
(5) Integrated in 5MHz bandwidth
(6) For Bluetooth sensitivity of -67dBm with 0.1% BER

5.2 Temperature -40°C

5.2.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = -40°C					
	Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power(1)	4	8	-	-6 to +4(2)	dBm
RF power control range	25	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	820	1000	≤1000	kHz
Adjacent channel transmit power $F=F_0 \pm 2MHz$(3) (4)	-	-35	-20	≤-20	dBm
Adjacent channel transmit power $F=F_0 \pm 3MHz$(3) (4)	-	-45	-40	≤-40	dBm
Δf1avg "Maximum Modulation"	140	165	175	$140<\Delta f1_{avg}<175$	kHz
Δf2max "Minimum Modulation"	115	135	-	115	kHz
Δf2avg / Δf2avg	0.8	0.9	-	≥0.80	-
Initial carrier frequency tolerance	-	10	35	±75	kHz
Drift Rate	-	8	25	≤25	kHz/50μs
Drift (single slot packet)	-	9	25	≤25	kHz
Drift (five slot packet)	-	10	40	≤40	kHz

Notes:

(1) BlueCore2-ROM firmware maintains the transmit power to be within the Bluetooth specification v1.1 limits

(2) Class 2 RF transmit power range, Bluetooth specification v1.1

(3) Measured at F_0 = 2441MHz

(4) Up to three exceptions are allowed in v1.1 of the Bluetooth specification

5.2.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = -40°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER	2.402	-	-86.0	-81	≤-70	dBm
	2.441	-	-88.0	-82		
	2.480	-	-86.5	-82		
Maximum received signal at 0.1% BER		-2	1	-	≥-20	dBm

5.3 Temperature -25°C

5.3.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = -25°C					
	Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power(1)	3.5	7	-	-6 to +4(2)	dBm
RF power control range	25	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	820	1000	≤1000	kHz
Adjacent channel transmit power F=F_0 ±2MHz(3) (4)	-	-35	-20	≤-20	dBm
Adjacent channel transmit power F=F_0 ±3MHz(3) (4)	-	-45	-40	≤-40	dBm
Δf1avg "Maximum Modulation"	140	165	175	140<$\Delta f1_{avg}$<175	kHz
Δf2max "Minimum Modulation"	115	140	-	115	kHz
Δf2avg / Δf2avg	0.8	0.9	-	≥0.80	-
Initial carrier frequency tolerance	-	10	35	±75	kHz
Drift Rate	-	8	20	≤25	kHz/50µs
Drift (single slot packet)	-	9	20	≤25	kHz
Drift (five slot packet)	-	10	25	≤40	kHz

Notes:

(1) BlueCore2-ROM firmware maintains the transmit power to be within the Bluetooth specification v1.1 limits

(2) Class 2 RF transmit power range, Bluetooth specification v1.1

(3) Measured at F_0 = 2441MHz

(4) Up to three exceptions are allowed in v1.1 of the Bluetooth specification

5.3.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = -25°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER	2.402	-	-85.5	-81	≤-70	dBm
	2.441	-	-86.5	-82		
	2.480	-	-86.5	-82		
Maximum received signal at 0.1% BER		-2	1	-	≥-20	dBm

5.4 Temperature +85°C

5.4.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +85°C					
	Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power(1)	0	3	-	-6 to +4(2)	dBm
RF power control range	25	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	820	1000	≤1000	kHz
Adjacent channel transmit power $F=F_0 \pm 2MHz$(3) (4)	-	-35	-20	≤-20	dBm
Adjacent channel transmit power $F=F_0 \pm 3MHz$(3) (4)	-	-45	-40	≤-40	dBm
Δf1avg "Maximum Modulation"	140	165	175	$140<\Delta f1_{avg}<175$	kHz
Δf2max "Minimum Modulation"	115	140	-	115	kHz
Δf2avg / Δf2avg	0.8	0.9	-	≥0.80	-
Initial carrier frequency tolerance	-	10	35	±75	kHz
Drift Rate	-	9	20	≤25	kHz/50µs
Drift (single slot packet)	-	9	20	≤25	kHz
Drift (five slot packet)	-	10	28	≤40	kHz

Notes:

(1) BlueCore2-ROM firmware maintains the transmit power to be within the Bluetooth specification v1.1 limits

(2) Class 2 RF transmit power range, Bluetooth specification v1.1

(3) Measured at F_0 = 2441MHz

(4) Up to three exceptions are allowed in v1.1 of the Bluetooth specification

5.4.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = +85°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER	2.402	-	-81	-77	≤-70	dBm
	2.441	-	-83	-79		
	2.480	-	-83	-79		
Maximum received signal at 0.1% BER		0	5	-	≥-20	dBm

5.5 Temperature +105°C

5.5.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +105°C					
	Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power(1)	-2.5	1	-	-6 to +4(2)	dBm
RF power control range	25	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	820	1000	≤1000	kHz
Adjacent channel transmit power F=F_0 ±2MHz(3) (4)	-	-35	-20	≤-20	dBm
Adjacent channel transmit power F=F_0 ±3MHz(3) (4)	-	-45	-40	≤-40	dBm
Δf1avg "Maximum Modulation"	140	165	175	140<$\Delta f1_{avg}$<175	kHz
Δf2max "Minimum Modulation"	-	135	-	115	kHz
Δf2avg / Δf2avg	-	0.9	-	≥0.80	-
Initial carrier frequency tolerance	-	10	35	±75	kHz
Drift Rate	-	9	25	≤25	kHz/50µs
Drift (single slot packet)	-	9	25	≤25	kHz
Drift (five slot packet)	-	10	40	≤40	kHz

Notes:

(1) BlueCore2-ROM firmware maintains the transmit power to be within the Bluetooth specification v1.1 limits

(2) Class 2 RF transmit power range, Bluetooth specification v1.1

(3) Measured at F_0 = 2441MHz

(4) Up to three exceptions are allowed in v1.1 of the Bluetooth specification

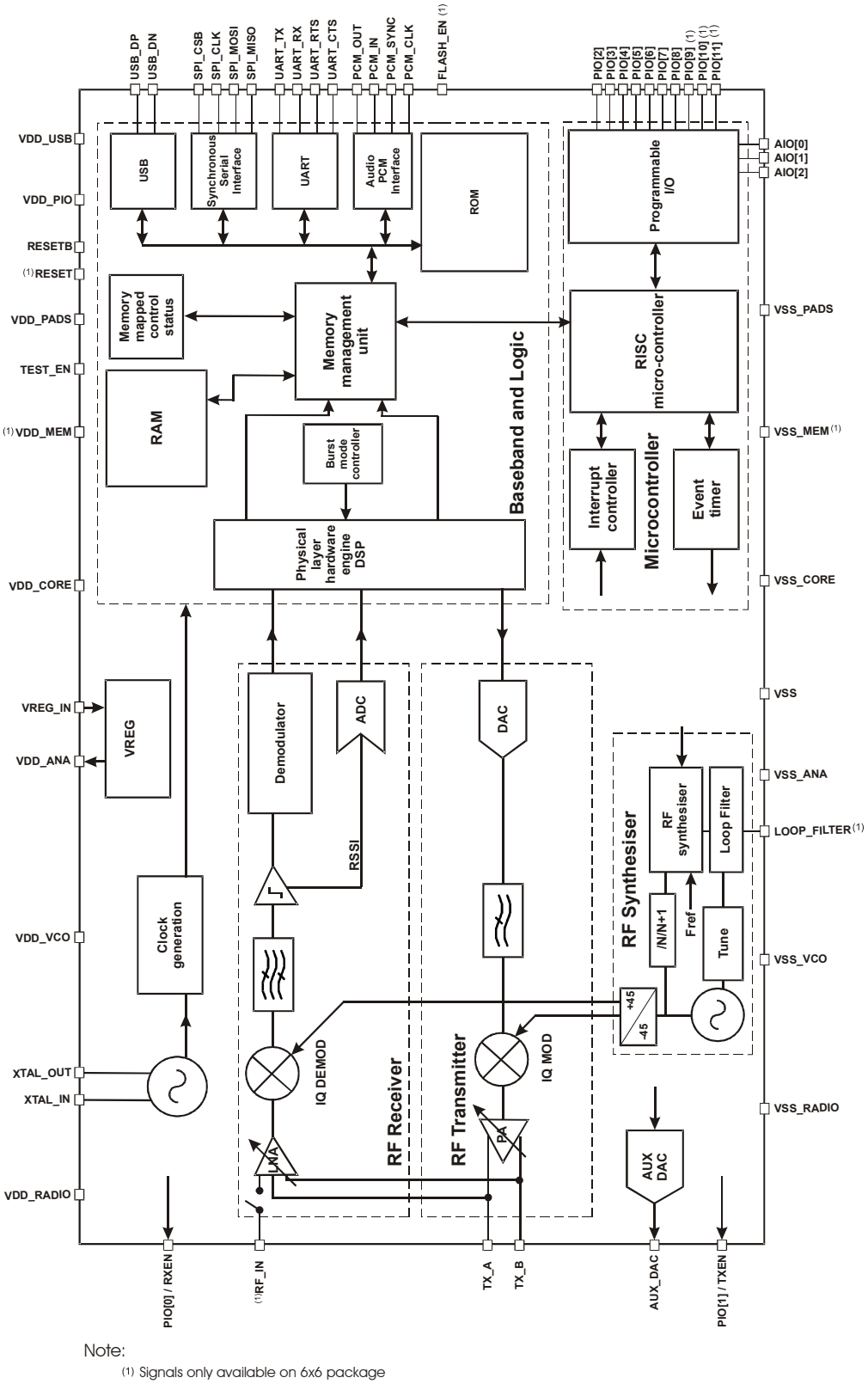
5.5.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = +105°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER	2.402	-	-81	-77	≤-70	dBm
	2.441	-	-82	-78		
	2.480	-	-82	-78		
Maximum received signal at 0.1% BER		0	5	-	≥-20	dBm

5.6 Power Consumption

Mode	Average	Unit
SCO connection HV3 (30ms interval Sniff Mode) (Slave)	26.0	mA
SCO connection HV3 (30ms interval Sniff Mode) (Master)	26.0	mA
SCO connection HV3 (No Sniff Mode) (Slave)	32.0	mA
SCO connection HV1 (Slave)	43.0	mA
SCO connection HV1 (Master)	43.0	mA
ACL data transfer 115.2kbps UART no traffic (Master)	7.0	mA
ACL data transfer 115.2kbps UART no traffic (Slave)	24.0	mA
ACL data transfer 720kbps UART (Master or Slave)	50.0	mA
ACL data transfer 720kbps USB (Master or Slave)	50.0	mA
ACL connection, Sniff Mode 40ms interval, 38.4kbps UART	4.0	mA
ACL connection, Sniff Mode 1.28s interval, 38.4kbps UART	0.5	mA
Parked Slave, 1.28s beacon interval, 38.4kbps UART	0.6	mA
Standby Mode (Connected to host, no RF activity)	85.0	µA
Reset (RESET high or RESETB low)	50.0	µA

6 Device Diagrams



Note:
(1) Signals only available on 6x6 package

Figure 6.1: BlueCore2-ROM Device Diagram for 6 x 6mm VFBGA and 4 x 4mm CSP Packages

7 Description of Functional Blocks

7.1 RF Receiver

The receiver features a near zero Intermediate Frequency (IF) architecture that allows the channel filters to be integrated on to the die. Sufficient out of band blocking specification at the Low Noise Amplifier (LNA) input allows the radio to be used in close proximity to Global System for Mobile Communications (GSM) and Wideband Code Division Multiple Access (W-CDMA) cellular phone transmitters without being desensitised. The use of a digital Frequency Shift Keying (FSK) discriminator means that no discriminator tank is needed, and its excellent performance in the presence of noise allows BlueCore2-ROM to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

7.1.1 Low Noise Amplifier

The LNA can be configured to operate in single ended or differential mode. Single ended mode is used for Class 1 Bluetooth operation and differential mode is used for Class 2 operation.

7.1.2 Analogue to Digital Converter

The analogue to digital converter (ADC) is used to implement fast automatic gain control (AGC). The ADC samples the Received Signal Strength Indicator (RSSI) voltage on a slot by slot basis. The front end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

7.2 RF Transmitter

7.2.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise the frequency drift during a transmit timeslot which results in a controlled modulation index. A digital baseband transmit filter provides the required spectral shaping.

7.2.2 Power Amplifier

The internal power amplifier (PA) has a maximum output power of +6dBm allowing BlueCore2-ROM to be used in Class 2 and Class 3 radios without an external RF PA. Support for transmit power control allows a simple implementation for Class 1 with an external RF PA.

7.2.3 Auxiliary DAC

An 8-bit voltage Auxiliary DAC is provided for power control of an external PA for Class 1 operation.

7.3 RF Synthesiser

The radio synthesiser is fully integrated onto the die with no requirement for an external voltage controlled oscillator (VCO) screening can, varactor tuning diodes, LC resonators or loop filter.

7.4 Clock Input and Generation

The reference clock for the system is generated from a TCXO or crystal input between 8 and 40MHz. All internal reference clocks are generated using a phase locked loop (PLL), which is locked to the external reference frequency.

7.5 Baseband and Logic

7.5.1 Memory Management Unit

The memory management unit (MMU) provides a number of dynamically allocated ring buffers that hold the data which is in transit between the host and the air or vice versa. The dynamic allocation of memory ensures efficient use of the available random access memory (RAM) and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

7.5.2 Burst Mode Controller

During radio transmission the burst mode controller (BMC) constructs a packet from header information previously loaded into memory mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During radio reception, the BMC stores the packet header in memory mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

7.5.3 Physical Layer Hardware Engine DSP

Dedicated logic is used to perform the following:

- Forward error correction (FEC)
- Header error control (HEC)
- Cyclic redundancy check (CRC)
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding
- The following voice data translations and operations are performed by firmware:
  - A-law/μ-law/linear voice data from host
  - A-law/μ-law/Continuously Variable Slope Delta (CVSD) over the air
  - Voice interpolation for lost packets
  - Rate mismatches

7.5.4 RAM

32Kbytes of on chip RAM is provided and is shared between the ring buffers used to hold voice/data for each active connection and the general purpose memory required by the Bluetooth stack.

7.5.5 ROM

4Mbits of metal programmable ROM is provided for system firmware implementation.

7.5.6 USB

This is a full speed universal serial bus (USB) interface for communicating with other compatible digital devices. BlueCore2-ROM acts as a USB peripheral, responding to requests from a Master host controller such as a PC.

7.5.7 Synchronous Serial Interface

This is a synchronous serial port interface (SPI) for interfacing with other digital devices. The SPI port can be used for system debugging.

7.5.8 UART

This is a standard Universal Asynchronous Receiver Transmitter (UART) interface for communicating with other serial devices.

7.5.9 Audio PCM Interface

The audio pulse code modulation (PCM) Interface supports continuous transmission and reception of PCM encoded audio data over Bluetooth.

7.6 Microcontroller

The microcontroller, interrupt controller and event timer run the Bluetooth software stack and control the radio and host interfaces. A 16-bit reduced instruction set computer (RISC) microcontroller is used for low power consumption and efficient use of memory.

7.6.1 Programmable I/O

BlueCore2-ROM has up to 15 (12 digital and 3 analogue) programmable I/O terminals. These are controlled by firmware running on the device.

8 CSR Bluetooth Software Stacks

8.1 Important Information

Due to the nature of a ROM device the initial boot configuration of CSR's generic ROM part is fixed to a predetermined default configuration. Areas covered include clock frequency, host transport, baud rate, persistent store values, etc.

To reconfigure the device to meet a design's requirements the PIO lines are read during the initial cold boot procedure and the device is reprogrammed accordingly. These new settings are activated after sending a warm reset to the device.

For details of the implementation and the PIO line configurations please refer to latest software release note.

BlueCore2-ROM is supplied with Bluetooth stack firmware which runs on the internal RISC microcontroller. This is compliant with the Bluetooth specification v1.1.

The BlueCore2-ROM software architecture allows Bluetooth processing overheads to be shared in different ways between the internal RISC microcontroller and the host processor. The upper layers of the Bluetooth stack (above HCI) can be run either on chip or on the host processor.

Running the upper stack on BlueCore2-ROM reduces or eliminates in the case of a virtual machine (VM) application, the need for host side software and processing time. Running the upper layers on the host processor allows greater flexibility.

8.2 BlueCore HCI Stack

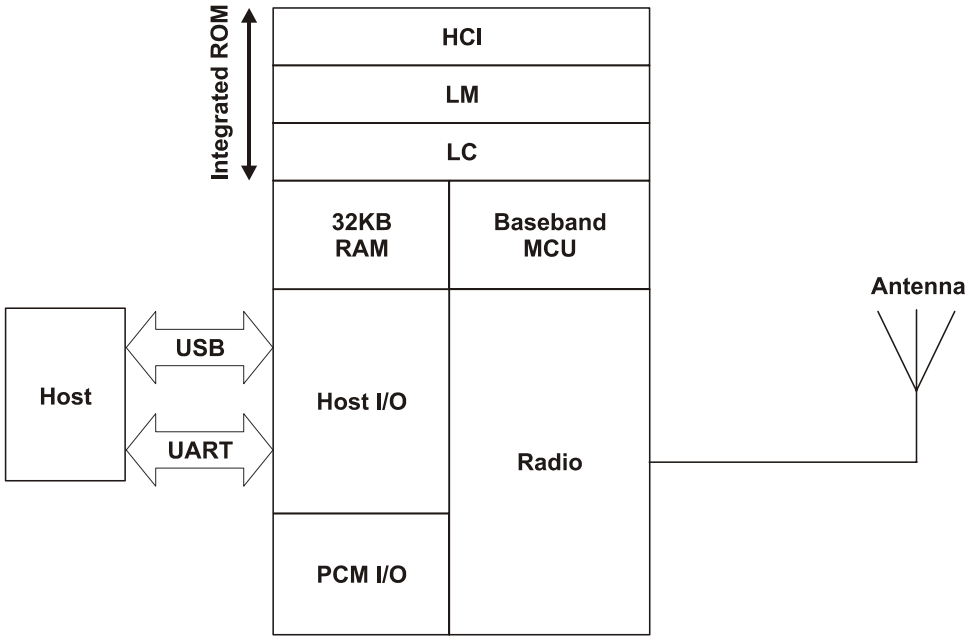


Figure 8.1: BlueCore HCI Stack

In the implementation shown in Figure 8.1, the internal processor runs the Bluetooth stack up to the Host Controller Interface (HCI). All upper layers must be provided by the Host processor.

8.2.1 Key Features of the HCI Stack

Standard Bluetooth Functionality

- The firmware has been written against the Bluetooth Core Specification v1.1
- Bluetooth components: Baseband (including LC), LM and HCI
- Standard USB v1.1 and UART (H4) HCI transport layers
- All standard radio packet types
- Full Bluetooth data rate, up to 723.2kb/s asymmetric (1)
- Operation with up to 7 active slaves (1)
- Maximum number of simultaneous active ACL connections: 7(2)
- Maximum number of simultaneous SCO connections: 3(2)
- Operation with up to 3 SCO links, routed to one or more slaves
- Role switch: can reverse Master/Slave relationship
- All standard SCO voice codings, plus “transparent SCO”
- Standard operating modes: page, inquiry, page-scan and inquiry-scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanisms: Hold, Sniff and Park modes, including Forced Hold
- Dynamic control of peers’ transmit power via LMP
- Master/Slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth test modes

The firmware’s supported Bluetooth features are detailed in the standard Protocol Implementation Conformance Statement (PICS) documents, available from www.csrsupport.com.

Notes:

(1) Maximum allowed by Bluetooth specification v1.1

(2) BlueCore2-ROM supports all combinations of active ACL and SCO channels for both Master and Slave operation, as specified by the Bluetooth specification v1.1

Extra Functionality

The firmware extends the standard Bluetooth functionality with the following features:

- Supports BlueCore serial protocol (BCSP), a proprietary, reliable alternative to the standard Bluetooth H4 UART Host Transport
- Provides a set of approximately 50 manufacturer-specific HCI extension commands. This command set, called BCCMD (BlueCore Command), provides:
  - Access to the device's general-purpose PIO port
  - Access to the device's Bluetooth clock (this can help transfer connections to other Bluetooth devices)
  - The negotiated effective encryption key length on established Bluetooth links
  - Access to the firmware's random number generator
  - Controls to set the default and maximum transmit powers e.g. These can help minimise interference between overlapping, fixed-location piconets
  - Dynamic UART configuration
  - Radio transmitter enable/disable e.g. A simple command connects to a dedicated hardware switch that determines whether the radio can transmit
- The firmware can read the voltage on a pair of the chip's external pins e.g. This is normally used to build a battery monitor, using either VM or host code.
- A block of BCCMD commands provides access to the chip's Persistent Store configuration database. The database sets the device's Bluetooth address, Class of device, radio (transmit class) configuration, SCO routing, LM and USB.
- A UART break condition can be used in three ways:
  - Presenting a UART break condition to the chip can force the chip to perform a hardware reboot
  - Presenting a break condition at boot time can hold the chip in a low power state, preventing normal
  - initialisation while the condition exists
  - With BCSP, the firmware can be configured to send a break to the host before sending data normally used to wake the host from a deep sleep state
- A block of radio test or BIST commands allows direct control of the device's radio. This aids the development of modules' radio designs, and can be used to support Bluetooth qualification.
- Virtual Machine (VM). The firmware provides the VM environment in which to run application-specific code. Although the VM is mainly used with BlueLab™ and RFCOMM builds (alternative firmware builds providing L2CAP, SDP and RFCOMM), the VM can be used with this build to perform simple tasks such as flashing LEDs via the chip's PIO port.
- Hardware low power modes:
  - Shallow sleep
  - Deep sleep
- The device drops into modes that significantly reduce power consumption when the software goes idle.
- SCO channels are normally routed over HCI (over BCSP). However, a single SCO channel can be routed over the chip's single PCM port at the same time as routing up to two other SCO channels over HCI. Alternatively up to 3 SCO channels can be mapped to the PCM port.

8.3 BlueCore RFCOMM Stack

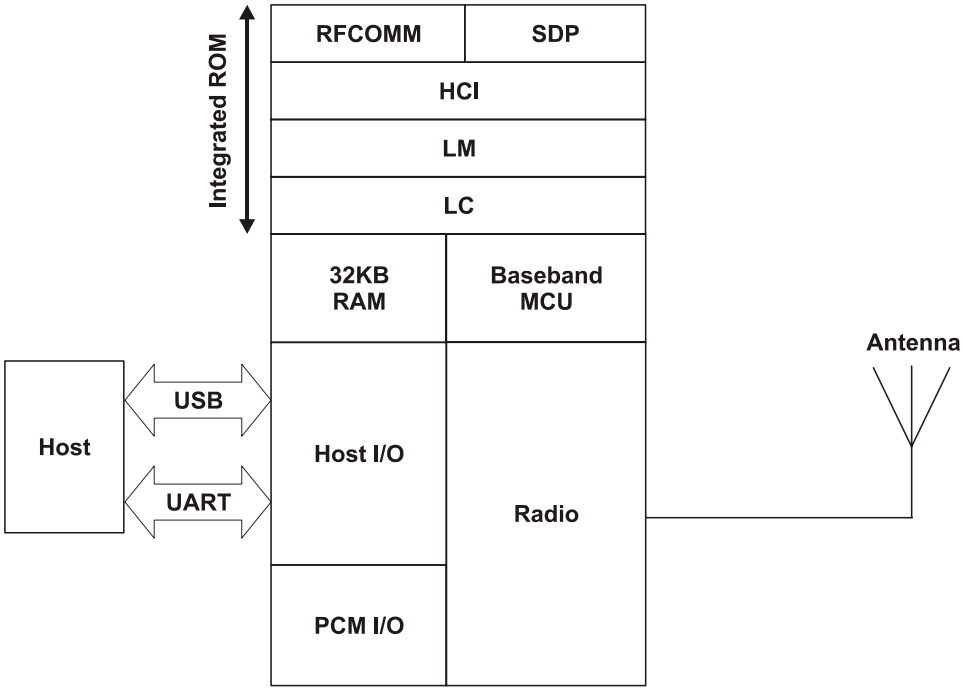


Figure 8.2: BlueCore RFCOMM Stack

In this version of the firmware the upper layers of the Bluetooth stack up to RFCOMM are run on chip. This reduces host side software and hardware requirements at the expense of some of the power and flexibility of the HCI only stack.

8.3.1 Key Features of the BlueCore2-ROM RFCOMM Stack

Interfaces to Host

- RFCOMM, an RS-232 serial cable emulation protocol
- SDP, a service database look-up protocol

Connectivity

- Maximum number of active slaves: 3
- Maximum number of simultaneous active ACL connections: 3
- Maximum number of simultaneous active SCO connections: 3
- Data Rate: up to 350Kb/s

Security

- Full support for all Bluetooth security features up to and including strong 128-bit encryption

Power Saving

- Full support for all Bluetooth power saving modes Park, Sniff and Hold

Data Integrity

- Channel quality driven data rate (CQDDR) increases the effective data rate in noisy environments.
- Receive signal strength indication (RSSI) used to minimise interference to other radio devices using the industrial, scientific and medical (ISM) band

8.4 BlueCore Virtual Machine Stack

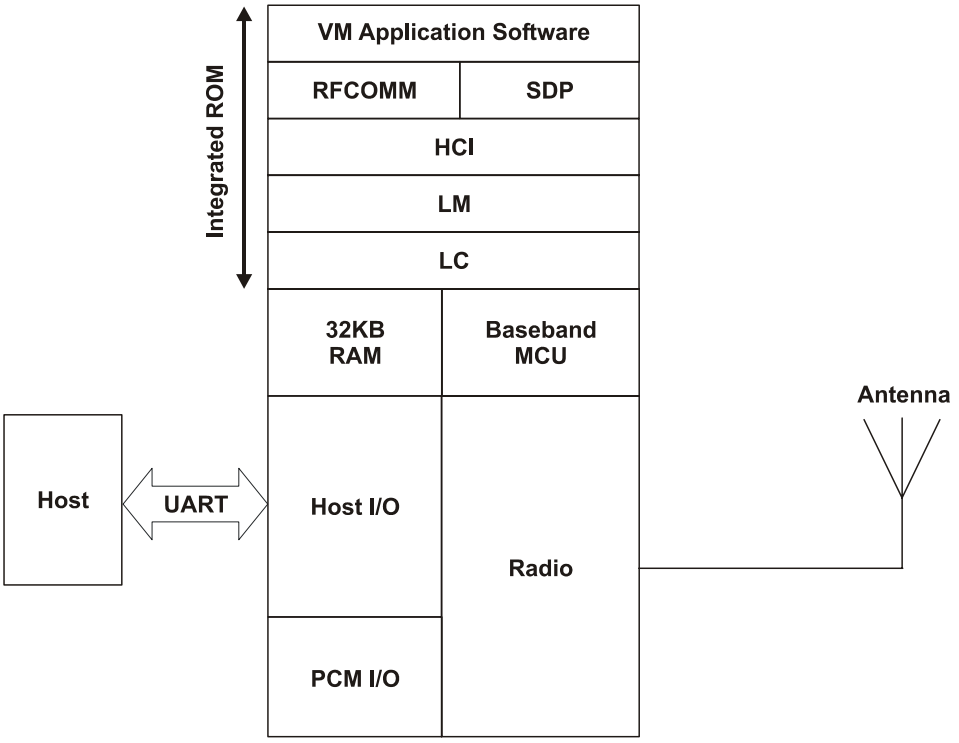


Figure 8.3: Virtual Machine

This version of the stack firmware requires no host processor. All software layers, including application software, run on the internal RISC microcontroller in a protected user software execution environment known as a virtual machine (VM).

The user may write custom application code to run on the BlueCore VM using BlueLab software development kit (SDK) supplied with the BlueLab and Casira™ development kits, available separately from CSR. This code will then execute alongside the main BlueCore firmware. The user is able to make calls to the BlueCore firmware for various operations.

The execution environment is structured so the user application does not adversely affect the main software routines, thus ensuring that the Bluetooth stack software component does not need re-qualification when the application is changed.

Using the VM and the BlueLab SDK the user is able to develop applications such as a cordless headset or other profiles without the requirement of a host controller. BlueLab is supplied with example code including a full implementation of the headset profile.[(1)]

On successful completion of firmware development and testing using BlueCore2-Flash (BC215159A), CSR can commit the code to a mask set for mass production of the device. A non recurring engineering (NRE) charge will be required.

Note:

Sample applications to control PIO lines can also be written with BlueLab SDK and the VM for the HCI stack.

(1) BlueLab Professional contains headset

8.5 BlueCore HID Stack

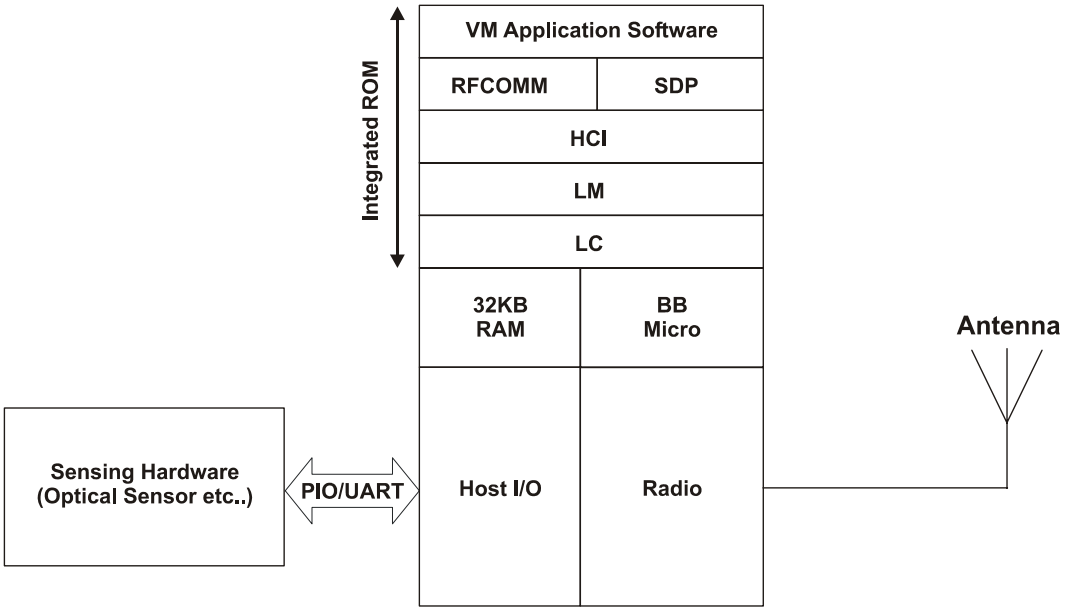


Figure 8.4: HID Stack

This version of the stack firmware requires no host processor. All software layers, including application software, run on the internal RISC microcontroller in a protected user software execution environment known as a virtual machine (VM).

The user may write custom application code to run on the BlueCore VM using BlueLab Professional software development kit (SDK) supplied with the BlueLab Professional and Casira development kits, available separately from CSR. This code will then execute alongside the main BlueCore firmware. The user is able to make calls to the BlueCore firmware for various operations.

The execution environment is structured so the user application does not adversely affect the main software routines, thus ensuring that the Bluetooth stack software component does not need re-qualification when the application is changed.

Using the VM and the BlueLab Professional SDK the user is able to develop Bluetooth HID devices such as an optical mouse or keyboard. The user is able to customise features such as power management and connect/reconnect behaviour.

The HID I/O component in the HID stack controls low latency data acquisition from external sensor hardware. With this component running in native code, it does not incur the overhead of the VM code interpreter. Supported external sensors include 5 mouse buttons, the Agilent ADNS-2030 optical sensor, quadrature scroll wheel, direct coupling to a keyboard matrix and a UART interface to custom hardware.

On successful completion of firmware development and testing using BlueCore2-Flash (BC215159A), CSR can commit the code to a mask set for mass production of the device. A non recurring engineering (NRE) charge will be required.

A reference schematic for implementing a three button, optical mouse with scroll wheel is available from CSR.

8.6 Host Side Software

BlueCore2-ROM can be ordered with companion host side software:

- BlueCore2-PC includes software for a full Windows® 98/ME, Windows 2000 or Windows XP Bluetooth host side stack together with chip hardware described in this document.
- BlueCore2-Mobile includes software for a full host side stack designed for modern ARM based mobile handsets together with chip hardware described in this document.

8.7 Additional Software for Other Embedded Applications

When the upper layers of the Bluetooth protocol stack are run as firmware on BlueCore2-ROM, a UART software driver is supplied that presents the L2CAP, RFCOMM and Service Discovery (SDP) APIs to higher Bluetooth stack layers running on the host. The code is provided as 'C' source or object code.

8.8 CSR Development Systems

CSR's BlueLab and Casira development kits are available to allow the evaluation of the BlueCore2 hardware and software, and as toolkits for developing on chip and host software.

9 Application Schematics

9.1 6 x 6 VFBGA 84-Ball Package

9.1.1 Application Schematic using Separate Balun and Filter

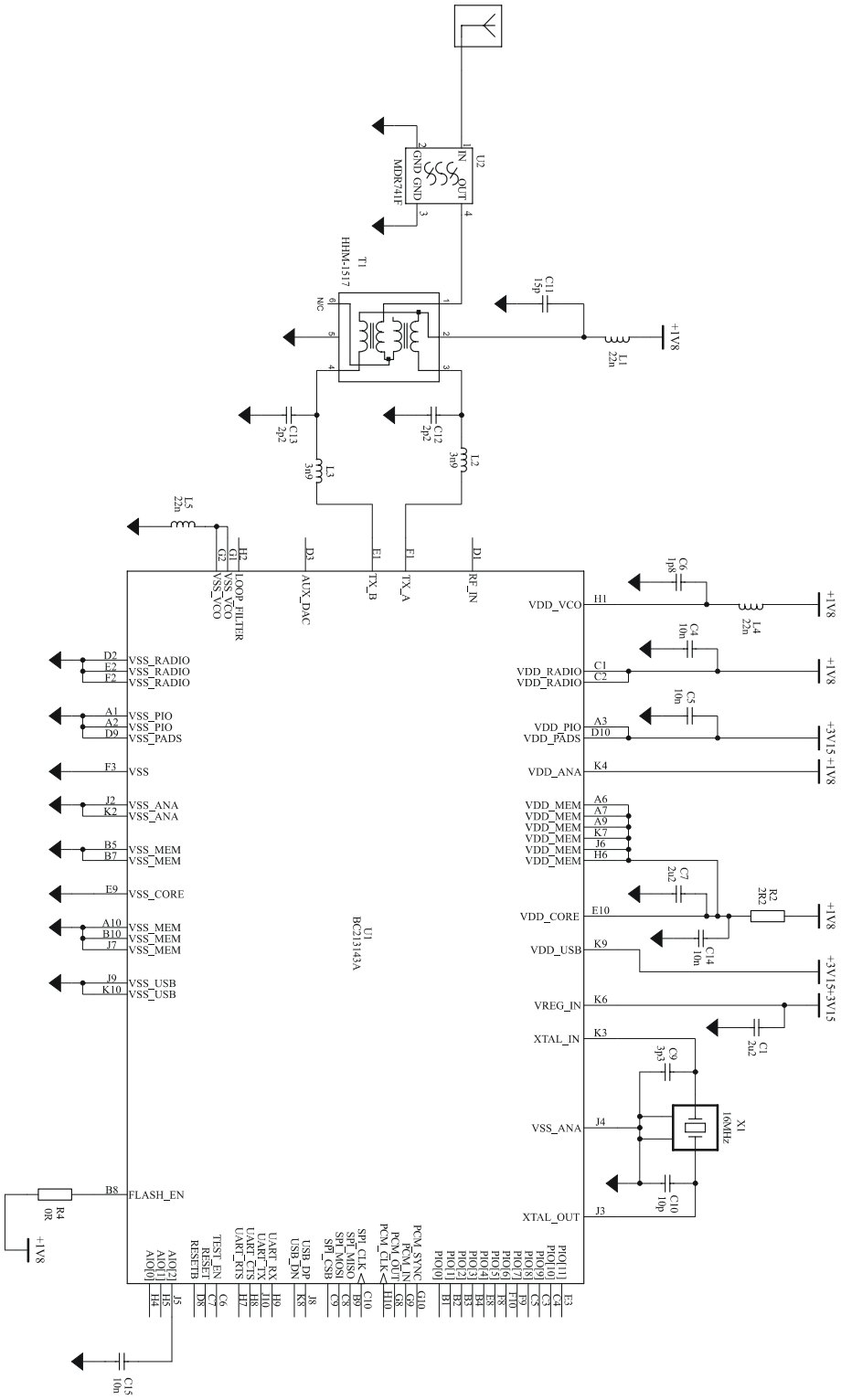


Figure 9.1: Application Circuit using Separate Balun and Filter for 6 x 6 VFBGA Package

9.1.2 Application Schematic using Epcos Combined Balun and Filter

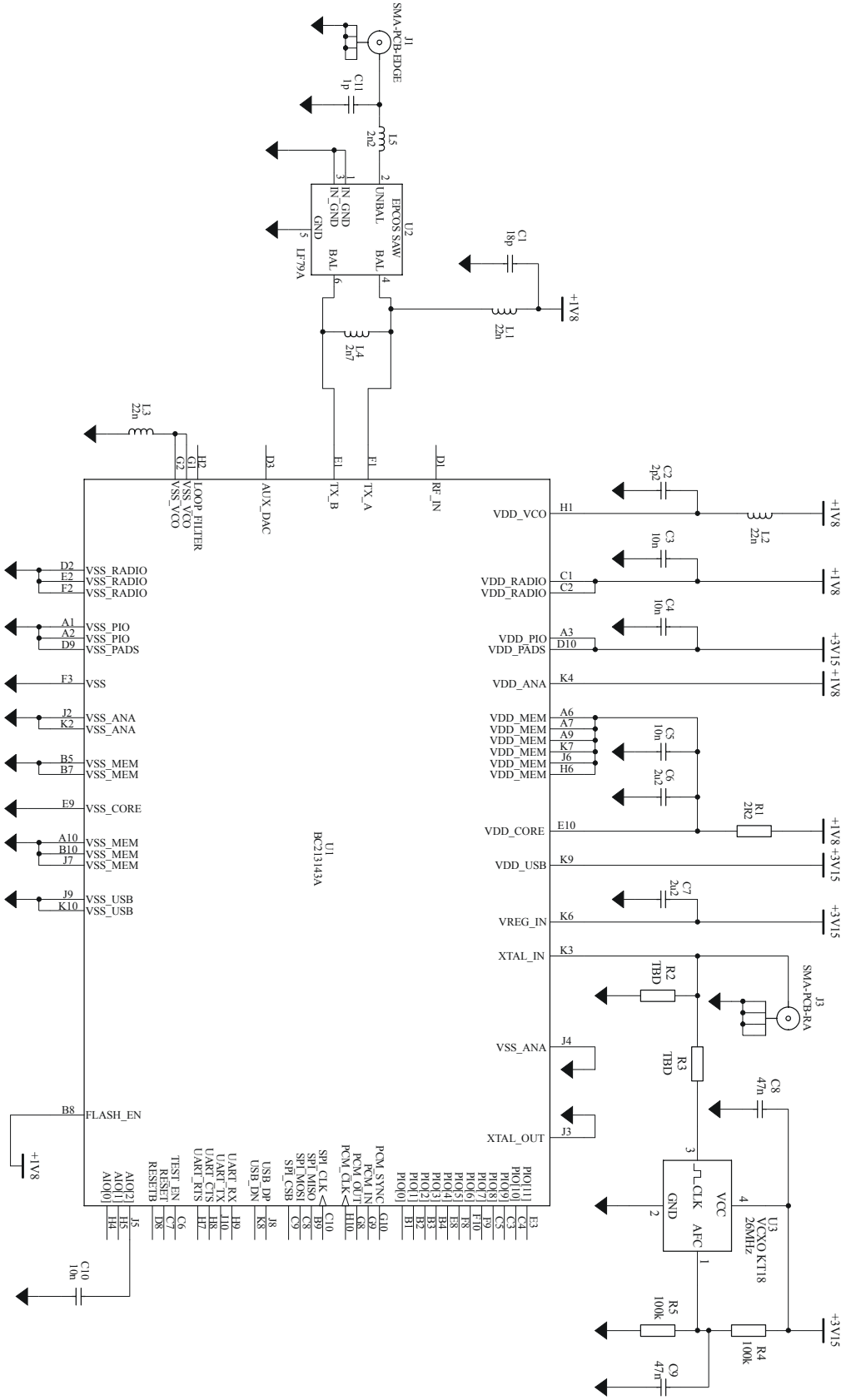


Figure 9.2: Application Circuit using Epcos Balun and Filter for 6 x 6 VFBGA Package

9.1.3 Application Schematic using Soshin Combined Balun and Filter

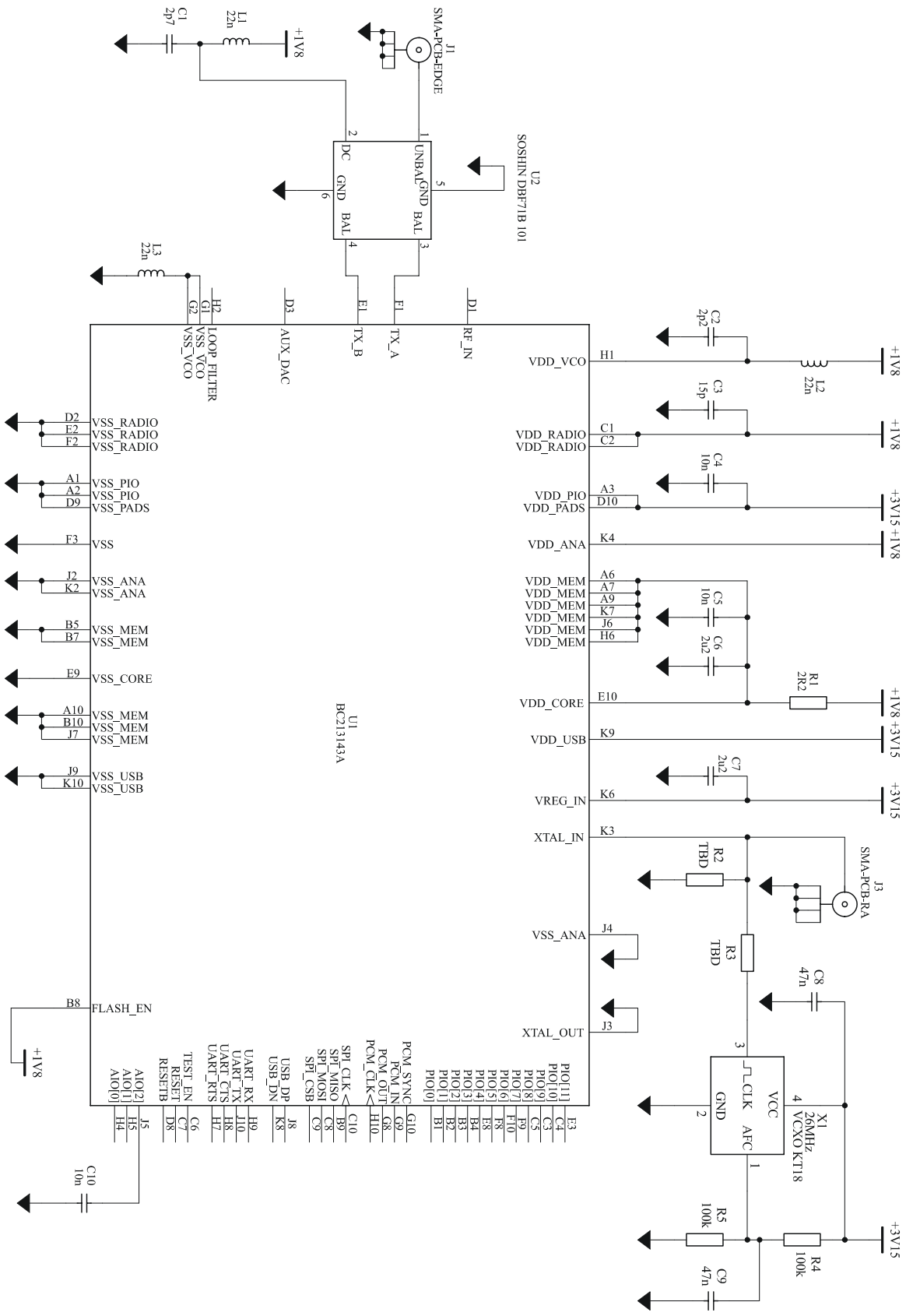


Figure 9.3: Application Circuit using Soshin Balun and Filter for 6 x 6 VFBGA Package

9.2 4 x 4 CSP 49-Ball Package

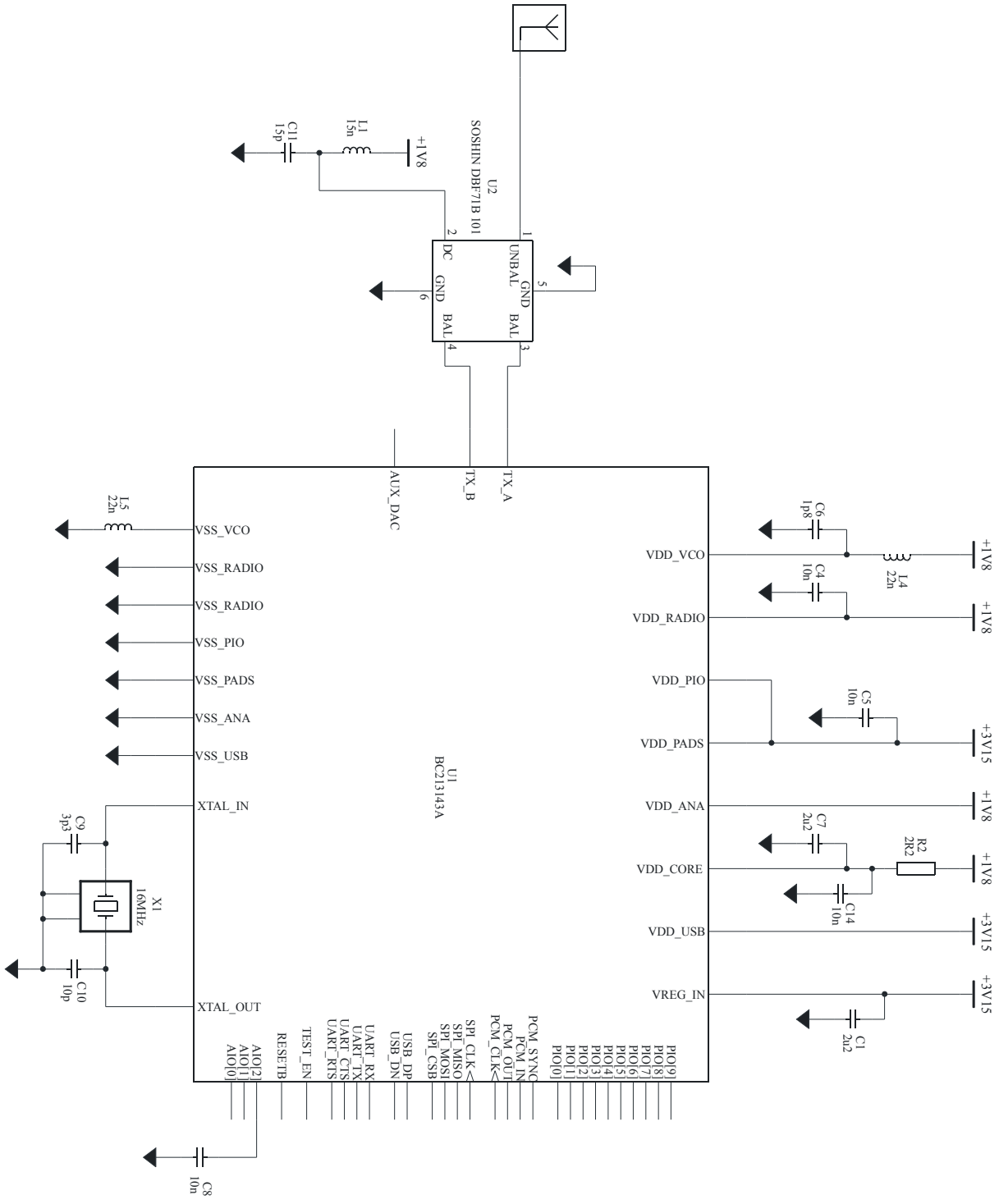
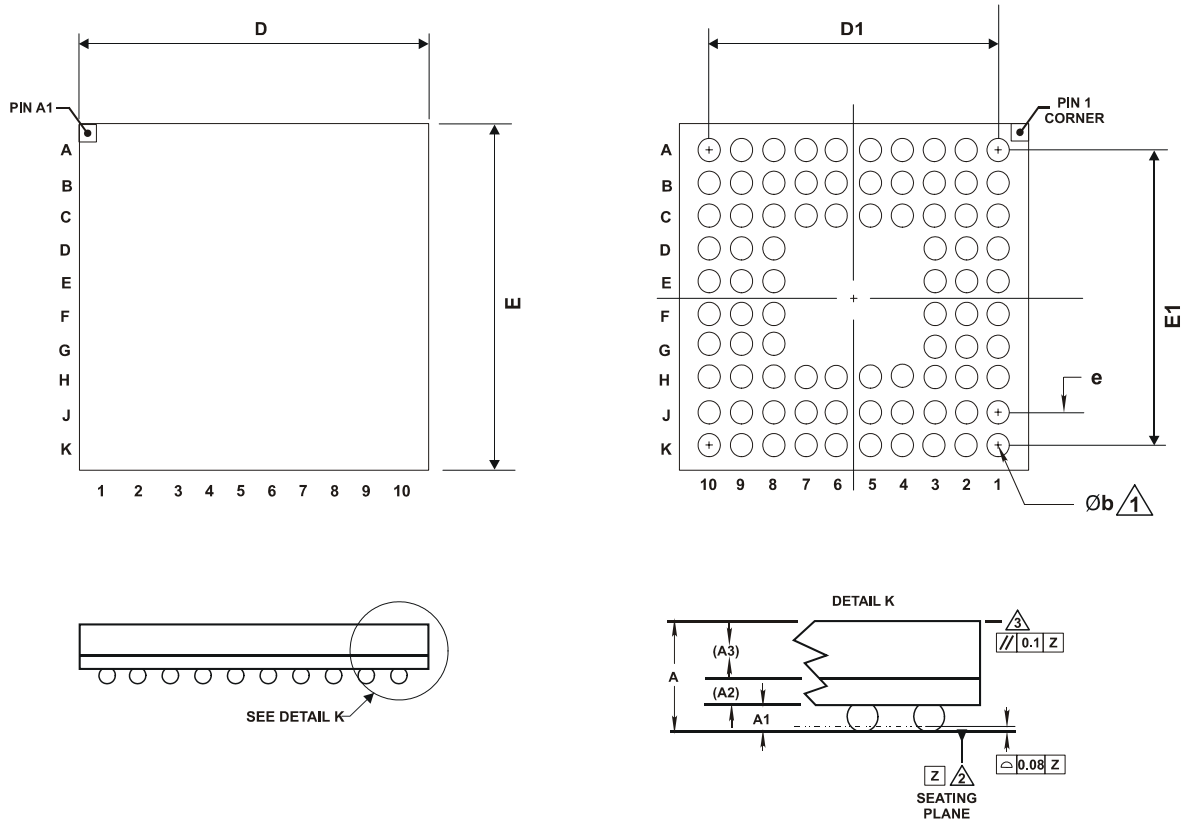


Figure 9.4: Application Circuit for 4 x 4 CSP Package

10 Package Dimensions

10.1 6 x 6 VFBGA 84-Ball Package

Top View **Bottom View**

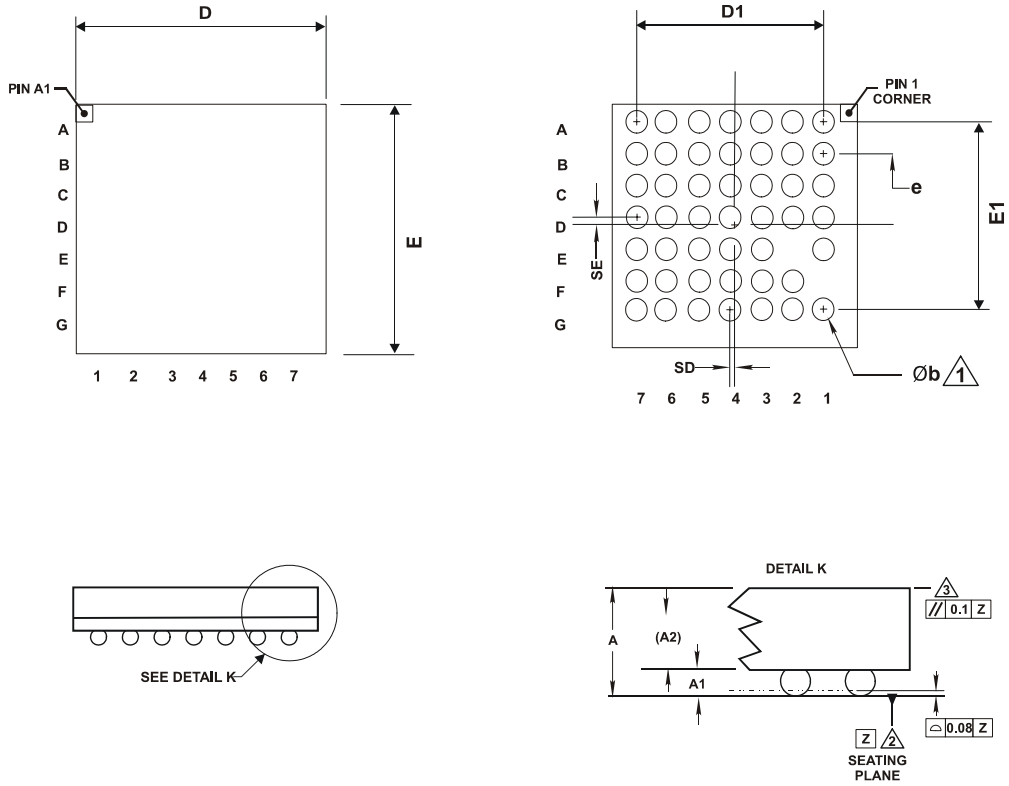


BC213143AXX-EK and BC213143AXX-RK 84-Ball 6x6x1mm VFBGA				
DIM	MIN	TYP	MAX	NOTES
A	0.8		1	1 DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM PLANE Z.
A1	0.2		0.3	
A2		0.22		
A3		0.45		2 DATUM Z IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
b	0.25	0.30	0.35	
D	5.90	6	6.10	
E	5.90	6	6.10	3 PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
e		0.50		
D1		4.50		
E1		4.50		
84-Ball VFBGA 6X6X1 mm (JEDEC MO-225)				UNIT: MM

Figure 10.1: BlueCore2-ROM VFBGA Package Dimensions

10.2 4 x 4 CSP 47-Ball Package

Top View **Bottom View**



BC213143AXX-XB 47-Ball 4.2 x 4.4 x 0.7mm CSP				
DIM	MIN	TYP	MAX	NOTES
A	0.55	0.57	0.70	
A1	0.21	0.24	0.27	
A2		0.33		
b	0.25	0.30	0.35	
D	4.10	4.20	4.30	
E	4.25	4.35	4.45	
e		0.50		
D1		3.00		
E1		3.00		
SD		0.04		
SE		0.10		

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM PLANE Z.
2. DATUM Z IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

47-Ball CSP 4.2 x 4.4 x 0.7mm (JEDEC MO-211)	UNIT
	MM

Figure 10.2: BlueCore2-ROM CSP Package Dimensions

11 Ordering Information

11.1 BlueCore2-ROM

Interface Version	Package			Order Number
	Type	Size	Shipment Method	
UART and USB	84-Ball VFBGA	6x6x1mm	Tape and reel	BC213143AXX-EK-E4
	84-Ball VFBGA (Pb free)	6x6x1mm	Tape and reel	BC213143AXX-RK-E4
	47-Ball CSP (Pb free)	4x4x0.7mm	Tape and reel	BC213143AXX-XB-E4

Note:

XX denotes firmware type and firmware version status. These are determined on a customer and project basis.

Minimum Order Quantity: 2kpcs Taped and Reeled

12 Contact Information

CSR U.S.
1651 N. Collins Blvd.
Suite 210
Richardson
TX75080
Tel: +1 (972) 238 2300
Fax: +1 (972) 231 1440
e-mail: sales@csr.com

CSR UK
Cambridge Science Park
Milton Road
Cambridge, CB4 0WH
United Kingdom
Tel: +44 (0) 1223 692 000
Fax: +44 (0) 1223 692 001
e-mail: sales@csr.com

CSR Denmark
Novi Science Park
Niels Jernes Vej 10
9220 Aalborg East
Denmark
Tel: +45 72 200 380
Fax: +45 96 354 599
e-mail: sales@csr.com

CSR Japan
9F Kojimachi KS Square 5-3-3,
Kojimachi, Chiyoda-ku,
Tokyo 102-0083
Japan
Tel: +81 3 5276 2911
Fax: +81 3 5276 2915
e-mail: sales@csr.com

CSR Singapore
Blk 5, Ang Mo Kio
Industrial Park 2A,
AMK Tech II, #07-08
Singapore 567760
Tel: +65 6484 2212
Fax: +65 6484 2219
e-mail: sales@csr.com

CSR Korea
Rm. 1111 Keumgang Venturetel,
#1108 Beesan-dong,
Dong An-ku, Anyang-city,
Kyunggi-do 431-050,
Korea
Tel: +82 31 389 0541
Fax : +82 31 389 0545
e-mail: sales@csr.com

To contact a CSR representative, go to http://www.csr.com/contacts.htm

13 Document References

Document:	Reference, Date:
Specification of the Bluetooth system	v1.1, 22 February 2001
Universal Serial Bus Specification	v1.1, 23 September 1998
I^2C EEPROMS for Use with BlueCore	CSR document bcore-an-008Pa, October 2002

Acronyms and Definitions

Term:	Definition:
BlueCore	Group term for CSR's range of Bluetooth chips.
Bluetooth	A set of technologies providing audio and data transfer over short-range radio connections
ACL	Asynchronous Connection-Less. A Bluetooth data packet.
AC	Alternating Current
ADC	Analogue to Digital Converter
AGC	Automatic Gain Control
A-law	Audio encoding standard
API	Application Programming Interface
ASIC	Application Specific Integrated Circuit
BCSP	BlueCore™ Serial Protocol
BER	Bit Error Rate. A measure of the quality of a link
BGA	Ball Grid Array
BIST	Built-In Self-Test
BOM	Bill of Materials. Component part list and costing for a product
BMC	Burst Mode Controller
C/I	Carrier Over Interferer
CMOS	Complementary Metal Oxide Semiconductor
CODEC	Coder Decoder
CPU	Central Processing Unit
CQDDR	Channel Quality Driven Data Rate
CSP	Chip Scale Package
CSR	Cambridge Silicon Radio
CTS	Clear to Send
CVSD	Continuous Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
dBm	Decibels relative to 1mW
DC	Direct Current
DFU	Device Firmware Upgrade
FSK	Frequency Shift Keying
GCI	General Circuit Interface. Standard synchronous 2B+D ISDN timing interface
GSM	Global System for Mobile communications
HCI	Host Controller Interface
IQ Modulation	In-Phase and Quadrature Modulation
IF	Intermediate Frequency
ISDN	Integrated Services Digital Network
ISM	Industrial, Scientific and Medical
ksamples/s	kilosamples per second
L2CAP	Logical Link Control and Adaptation Protocol (protocol layer)
LC	Link Controller
LCD	Liquid Crystal Display
LGA	Land Grid Array

LNA	Low Noise Amplifier
LSB	Least-Significant Bit
μ-law	Audio Encoding Standard
MMU	Memory Management Unit
MISO	Master In Serial Out
OHCI	Open Host Controller Interface
PA	Power Amplifier
PCB	Printed Circuit Board
PCM	Pulse Code Modulation. Refers to digital voice data
PIO	Parallel Input Output
PLL	Phase Lock Loop
ppm	parts per million
PS Key	Persistent Store Key
RAM	Random Access Memory
REF	Reference. Represents dimension for reference use only.
RF	Radio Frequency
RFCOMM	Protocol layer providing serial port emulation over L2CAP
RISC	Reduced Instruction Set Computer
rms	root mean squared
ROM	Read Only Memory
RSSI	Receive Signal Strength Indication
RTS	Ready To Send
RX	Receive or Receiver
SCO	Synchronous Connection-Oriented. Voice oriented Bluetooth packet
SDK	Software Development Kit
SDP	Service Discovery Protocol
SIG	Special Interest Group
SOC	System On Chip
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSL	Secure Sockets Layer
SUT	System Under Test
SW	Software
TBD	To Be Defined
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus or Upper Side Band (depending on context)
VCO	Voltage Controlled Oscillator
VFBGA	Very Fine Ball Grid Array
VM	Virtual Machine
W-CDMA	Wideband Code Division Multiple Access

Status Information

The status of this Data Sheet is Production Information.

Important Note:

Performance and characterisation data reported is not guaranteed for the CSP package option. All data should be regarded as Pre-Production Information with respect to the CSP package.

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Advance Information:

Information for designers on the target specification for a CSR product in development.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-Production Information:

Final pinout and mechanical dimensions. All electrical specifications may be changed by CSR without notice.

Production Information:

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

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While every care has been taken to ensure the accuracy of the contents of this document, CSR cannot accept responsibility for any errors.

Record of Changes

Date:	Revision	Reason for Change:
JANUARY 2002	a	Latest information for BlueCore2-ROM.
APRIL 2002	b	Addition of pinout information and specification updates.
APRIL 2002	c	Pin H6 now designated as VDD_MEM instead of not connected.
JULY 2002	d	Conversion to new document format.
JANUARY 2003	e	Latest package information for BlueCore2-ROM.
JUNE 2003	f	CSP package information updated.

BlueCore™2-ROM

Product Data Sheet

BC213143A-ds-001Pf

June 2003