



**W40S11-02**

## SDRAM Buffer - 2 DIMM (Mobile)

### Features

- Ten skew-controlled CMOS outputs (SDRAM0:9)
- Supports two SDRAM DIMMs
- Ideal for high-performance systems designed around Intel®'s latest Mobile chip set
- I<sup>2</sup>C Serial configuration interface
- Skew between any two outputs is less than 250 ps
- 1 to 5 ns propagation delay
- DC to 133-MHz operation
- Single 3.3V supply voltage
- Low power CMOS design packaged in a 28-pin, 209-mil SSOP (Shrink Small Outline Package)

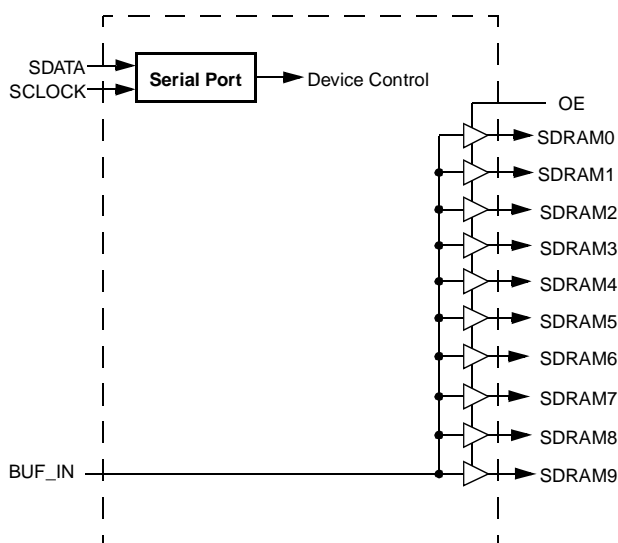
### Overview

The Cypress W40S11-02 is a low-voltage, ten-output clock buffer. Output buffer impedance is approximately 15Ω, which is ideal for driving SDRAM DIMMs.

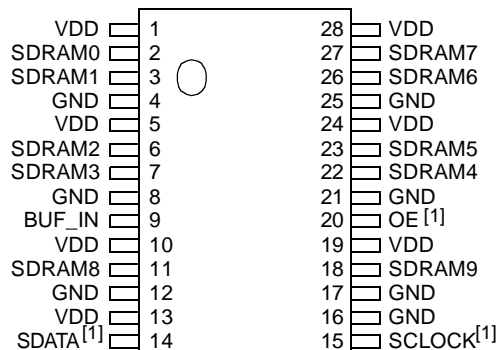
### Key Specifications

Supply Voltages:.....  $V_{DD} = 3.3V \pm 5\%$   
 Operating Temperature:..... 0°C to +70°C  
 Input Threshold: ..... 1.5V typical  
 Maximum Input Voltage: .....  $V_{DD} + 0.5V$   
 Input Frequency:..... 0 to 133 MHz  
 BUF\_IN to SDRAM0:9 Propagation Delay: ..... 1.0 to 5.0 ns  
 Output Edge Rate:.....  $\geq 1.5 V/ns$   
 Output Skew: .....  $\pm 250 ps$   
 Output Duty Cycle: ..... 45/55% worst case  
 Output Impedance:..... 15 ohms typical  
 Output Type: ..... CMOS rail-to-rail

### Block Diagram



### Pin Configuration



#### Note:

1. Internal pull-up resistor of 250K on SDATA, SCLOCK, and OE inputs (should not be relied upon for pulling up to  $V_{DD}$ ).

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**Pin Definitions**

Pin Name	Pin No.	Pin Type	Pin Description
SDRAM0:9	2, 3, 6, 7, 22, 23, 26, 27, 11, 18	O	<b>SDRAM Outputs:</b> Provides buffered copy of BUF_IN. The propagation delay from a rising input edge to a rising output edge is 1 to 5 ns. All outputs are skew controlled to within $\pm 250$ ps of each other.
BUF_IN	9	I	<b>Clock Input:</b> This clock input has an input threshold voltage of 1.5V (typ).
SDATA	14	I/O	<b>I<sup>2</sup>C Data Input:</b> Data should be presented to this input as described in the I <sup>2</sup> C section of this data sheet. Internal 250-k $\Omega$ pull-up resistor.
SCLOCK	15	I	<b>I<sup>2</sup>C Clock Input:</b> The I <sup>2</sup> C Data clock should be presented to this input as described in the I <sup>2</sup> C section of this data sheet. Internal 250-k $\Omega$ pull-up resistor.
VDD	1, 5, 10, 13, 19, 24, 28	P	<b>Power Connection:</b> Power supply for core logic and output buffers. Connected to 3.3V supply.
GND	4, 8, 12, 16, 17, 21, 25	G	<b>Ground Connection:</b> Connect all ground pins to the common system ground plane.
OE	20	I	<b>Output Enable:</b> Internal 250-k $\Omega$ pull-up resistor. Three-states outputs when LOW.

## Functional Description

### Output Control Pins

Outputs three-stated when OE = 0, and toggle when OE = 1. Outputs are in phase with BUF\_IN but are phase delayed by 1 to 5 ns. Outputs can also be controlled via the I<sup>2</sup>C interface.

### Output Drivers

The W40S11-02 output buffers are CMOS type which deliver a rail-to-rail (GND to V<sub>DD</sub>) output voltage swing into a nominal capacitive load. Thus, output signaling is both TTL and CMOS level compatible. Nominal output buffer impedance is 15 ohms.

### Operation

Data is written to the W40S11-02 in ten bytes of eight bits each. Bytes are written in the order shown in *Table 1*.

**Table 1. Byte Writing Sequence**

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the W40S11-02 to accept the bits in Data Bytes 0–6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the W40S11-02 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Don't Care	Unused by the W40S11-02, therefore bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	Don't Care	Unused by the W40S11-02, therefore bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	Refer to <i>Table 2</i>	The data bits in these bytes set internal W40S11-23 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to <i>Table 2</i> , Data Byte Serial Configuration Map.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3	Don't Care	Refer to Cypress clock drivers.
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6		

**Writing Data Bytes**

Each bit in the data bytes control a particular device function. Bits are written MSB (most significant bit) first, which is bit 7.

Table 2 gives the bit formats for registers located in Data Bytes 0–6.

**Table 2. Data Bytes 0–2 Serial Configuration Map<sup>[2]</sup>**

Bit(s)	Affected Pin		Control Function	Bit Control	
	Pin No.	Pin Name		0	1
Data Byte 0 SDRAM Active/Inactive Register (1=Enable, 0=Disable)					
7	N/A	Reserved	(Reserved)	--	--
6	N/A	Reserved	(Reserved)	--	--
5	N/A	Reserved	(Reserved)	--	--
4	N/A	Reserved	(Reserved)	--	--
3	7	SDRAM3	Clock Output Disable	Low	Active
2	6	SDRAM2	Clock Output Disable	Low	Active
1	3	SDRAM1	Clock Output Disable	Low	Active
0	2	SDRAM0	Clock Output Disable	Low	Active
Data Byte 1 SDRAM Active/Inactive Register (1=Enable, 0=Disable)					
7	27	SDRAM7	Clock Output Disable	Low	Active
6	26	SDRAM6	Clock Output Disable	Low	Active
5	23	SDRAM5	Clock Output Disable	Low	Active
4	22	SDRAM4	Clock Output Disable	Low	Active
3	N/A	Reserved	(Reserved)	--	--
2	N/A	Reserved	(Reserved)	--	--
1	N/A	Reserved	(Reserved)	--	--
0	N/A	Reserved	(Reserved)	--	--
Data Byte 2 SDRAM Active/Inactive Register (1=Enable, 0=Disable)					
7	18	SDRAM9	Clock Output Disable	Low	Active
6	11	SDRAM8	Clock Output Disable	Low	Active
5	N/A	Reserved	(Reserved)	--	--
4	N/A	Reserved	(Reserved)	--	--
3	N/A	Reserved	(Reserved)	--	--
2	N/A	Reserved	(Reserved)	--	--
1	N/A	Reserved	(Reserved)	--	--
0	N/A	Reserved	(Reserved)	--	--

**Note:**

- At power-up all SDRAM outputs are enabled and active. It is recommended to program Bits 4–7 of Byte0 and Bits 0–3 of Byte1 to a “0” to save power and reduce noise.

## How To Use the Serial Data Interface

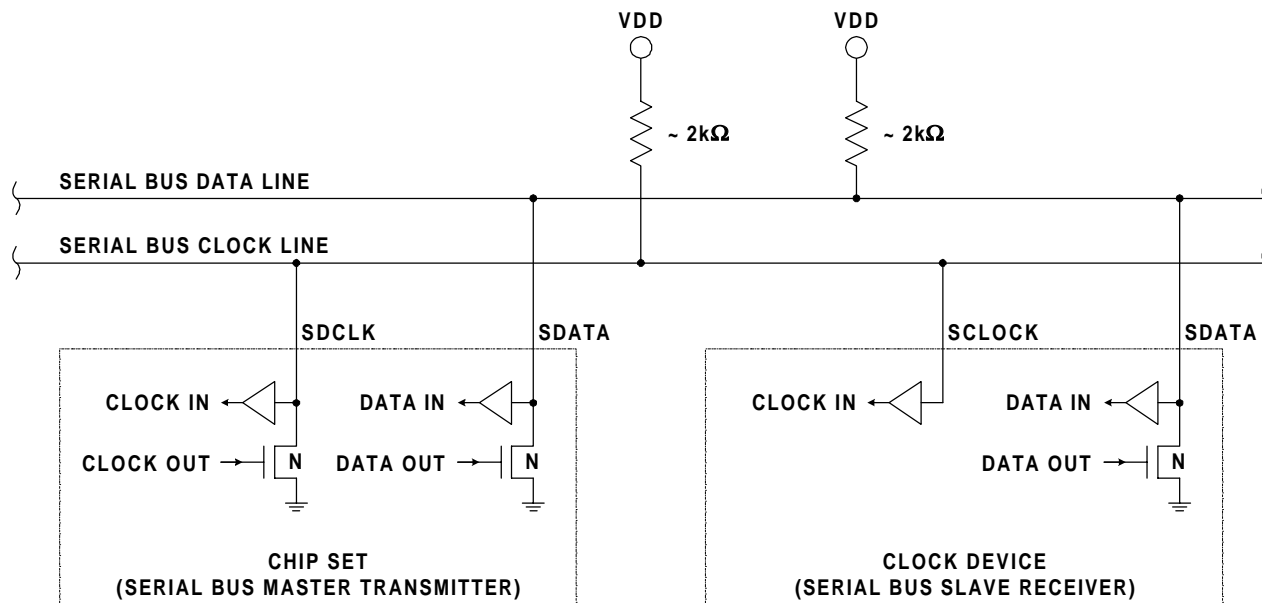
### Electrical Requirements

Figure 1 illustrates electrical characteristics for the serial interface bus used with the W40S11-02. Devices send data over the bus with an open drain logic output that can (a) pull the bus line LOW, or (b) let the bus default to logic 1. The pull-up resistor on the bus (both clock and data lines) establish a default

logic 1. All bus devices generally have logic inputs to receive data.

Although the W40S11-02 is a receive-only device (no data write-back capability), it does transmit an “acknowledge” data pulse after each byte is received. Thus, the SDATA line can both transmit and receive data.

The pull-up resistor should be sized to meet the rise and fall times specified in AC parameters, taking into consideration total bus line capacitance.



**Figure 1. Serial Interface Bus Electrical Characteristics**

### Signaling Requirements

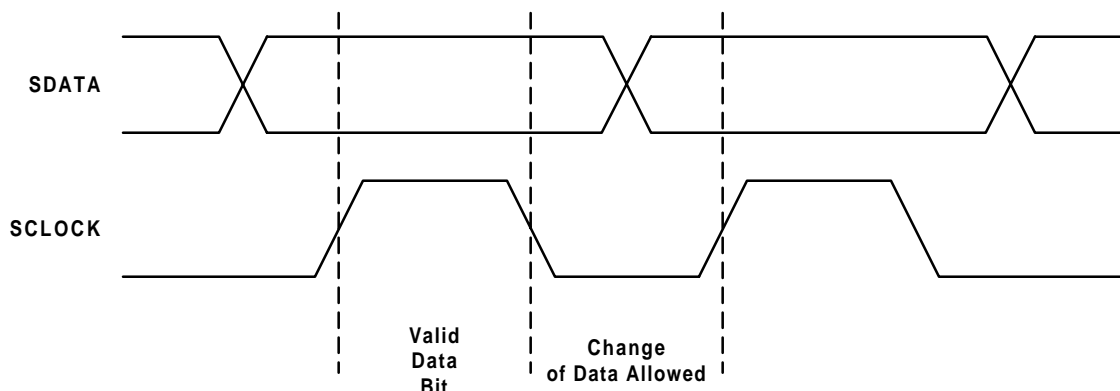
As shown in *Figure 2*, valid data bits are defined as stable logic 0 or 1 condition on the data line during a clock HIGH (logic 1) pulse. A transitioning data line during a clock HIGH pulse may be interpreted as a start or stop pulse (it will be interpreted as a start or stop pulse if the start/stop timing parameters are met).

A write sequence is initiated by a “start bit” as shown in *Figure 3*. A “stop bit” signifies that a transmission has ended.

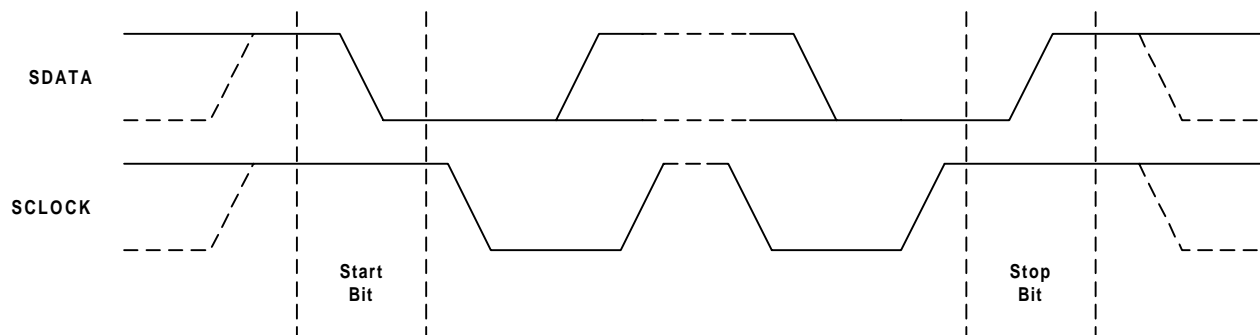
As stated previously, the W40S11-02 sends an “acknowledge” pulse after receiving eight data bits in each byte as shown in *Figure 4*.

### Sending Data to the W40S11-02

The device accepts data once it has detected a valid start bit and address byte sequence. Device functionality is changed upon the receipt of each data bit (registers are not double buffered). Partial transmission is allowed meaning that a transmission can be truncated as soon as the desired data bits are transmitted (remaining registers will be unmodified). Transmission is truncated with either a stop bit or new start bit (restart condition).



**Figure 2. Serial Data Bus Valid Data Bit**



**Figure 3. Serial Data Bus Start and Stop Bit**

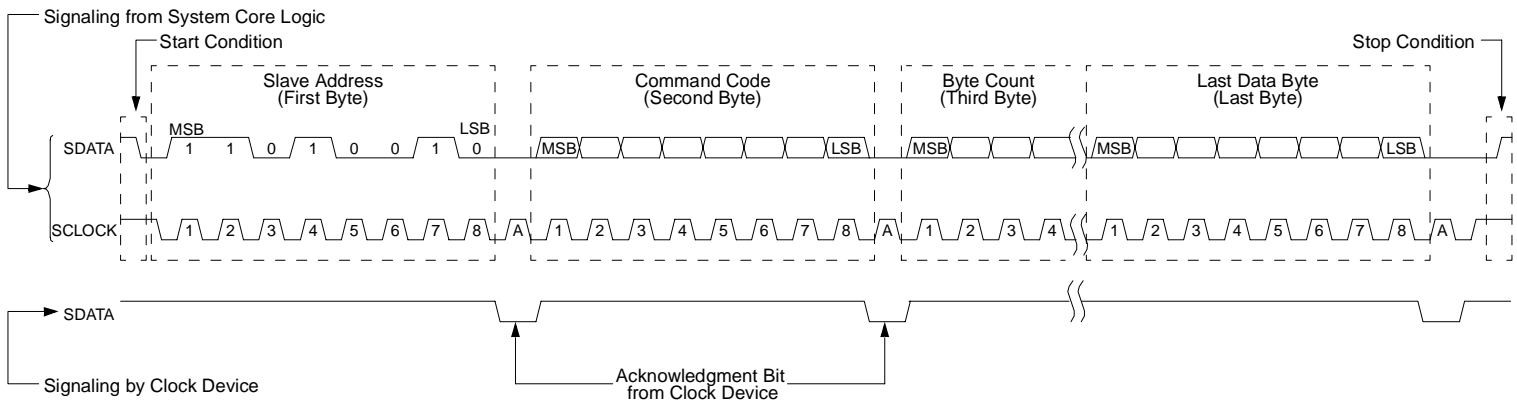


Figure 4. Serial Data Bus Write Sequence

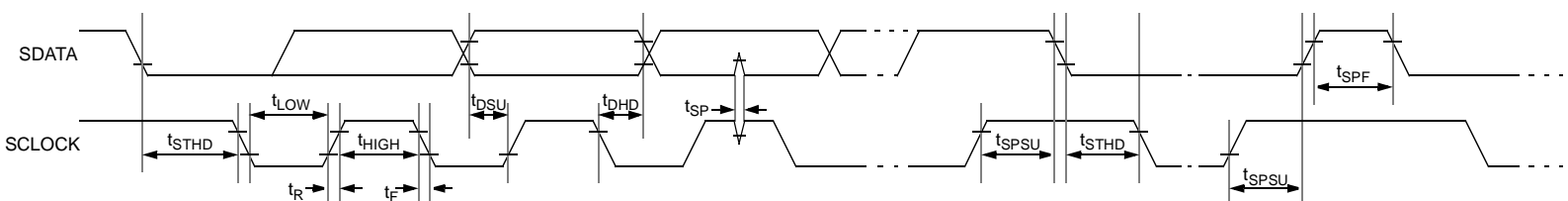


Figure 5. Serial Data Bus Timing Diagram

## Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions

above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
$V_{DD}, V_{IN}$	Voltage on any pin with respect to GND	-0.5 to +7.0	V
$T_{STG}$	Storage Temperature	-65 to +150	°C
$T_A$	Operating Temperature	0 to +70	°C
$T_B$	Ambient Temperature under Bias	-55 to +125	°C

## DC Electrical Characteristics: $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ , $V_{DD} = 3.3\text{V} \pm 5\%$

Parameter	Description	Test Condition/Comments	Min	Typ	Max	Unit
$I_{DD}$	3.3V Supply Current	at 66 MHz		120	160	mA
$I_{DD}$	3.3V Supply Current	at 100 MHz		185	220	mA
$I_{DD}$ Tristate	3.3V Supply Current in Three-State			5	10	mA
<b>Logic Inputs</b>						
$V_{IL}$	Input Low Voltage		$V_{SS}-0.3$		0.8	V
$V_{IH}$	Input High Voltage		2.0		$V_{DD}+0.5$	V
$I_{ILEAK}$	Input Leakage Current, BUF_IN		-5		+5	μA
$I_{ILEAK}$	Input Leakage Current <sup>[3]</sup>		-20		+5	μA
<b>Logic Outputs (SDRAM0:9)<sup>[4]</sup></b>						
$V_{OL}$	Output Low Voltage	$I_{OL} = 1\text{ mA}$			50	mV
$V_{OH}$	Output High Voltage	$I_{OH} = -1\text{ mA}$	3.1			V
$I_{OL}$	Output Low Current	$V_{OL} = 1.5\text{V}$	70	110	185	mA
$I_{OH}$	Output High Current	$V_{OH} = 1.5\text{V}$	65	100	160	mA
<b>Pin Capacitance/Inductance</b>						
$C_{IN}$	Input Pin Capacitance				5	pF
$C_{OUT}$	Output Pin Capacitance				6	pF
$L_{IN}$	Input Pin Inductance				7	nH

**Note:**

3. OE, SDATA, and SCLOCK logic pins have a 250-kΩ internal pull-up resistor ( $V_{DD} - 0.8\text{V}$ ).
4. All SDRAM outputs loaded by 6" transmission lines with 22-pF capacitors on ends.



**AC Electrical Characteristics:**  $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ,  $V_{DD} = 3.3\text{V} \pm 5\%$  (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition	Min	Typ	Max	Unit
$f_{IN}$	Input Frequency		0		133	MHz
$t_R$	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1.5		4.0	V/ns
$t_F$	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1.5		4.0	V/ns
$t_{SR}$	Output Skew, Rising Edges				250	ps
$t_{SF}$	Output Skew, Falling Edges				250	ps
$t_{EN}$	Output Enable Time		1.0		8.0	ns
$t_{DIS}$	Output Disable Time		1.0		8.0	ns
$t_{PR}$	Rising Edge Propagation Delay		1.0		5.0	ns
$t_{PF}$	Falling Edge Propagation Delay		1.0		5.0	ns
$t_D$	Duty Cycle	Measured at 1.5V	45		55	%
$Z_o$	AC Output Impedance			15		$\Omega$

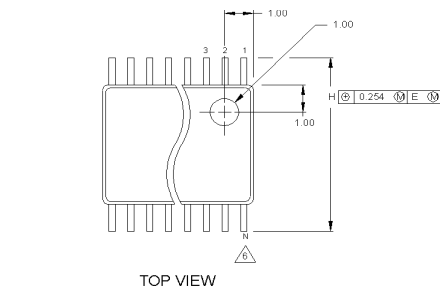
**Ordering Information**

Ordering Code	Freq. Mask Code	Package Name	Package Type
W40S11	-02	H X	28-pin SSOP (209-mil) 28-pin TSSOP (173-mil)

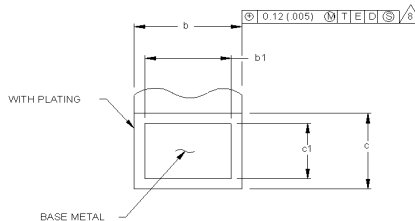
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## Package Diagrams

### 28-Pin Shrink Small Outline Package (TSSOP, 173-mil)

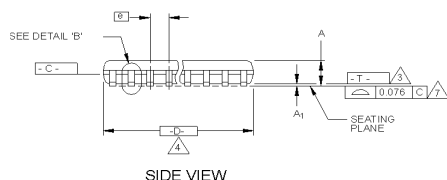


TOP VIEW

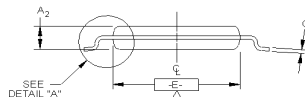


DETAIL "C"

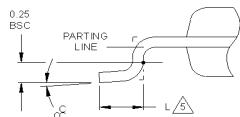
(SEE NOTE 9)



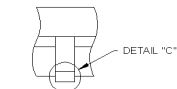
SIDE VIEW



END VIEW



DETAIL "A"  
(SCALE: 30/1)



DETAIL "B"  
(SCALE: 30/1)  
DAMBAR PROTRUSION

#### NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.279±0.0127 (0.110±0.005 INCHES)
2. DIMENSIONING & TOLERANCES PER ANSI Y14.5M-1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
5. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
6. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.076mm AT SEATING PLANE.
7. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND AN ADJACENT LEAD TO BE 0.14mm SEE DETAILS "B" AND "C".
8. DETAIL "C" TO BE DETERMINED AT 0.10 TO 0.25 MM FROM THE LEAD TIP.
9. CONTROLLING DIMENSION: MILLIMETERS.
10. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-153.
11. VARIATIONS AA, AB, AC, AD AND AE.

#### THIS TABLE IN MILLIMETERS

S V B O L	COMMON DIMENSIONS			N O T E	NOTE VARI- ATIONS	4 D			6 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A			1.10		AA	2.90	3.00	3.10	8
A <sub>1</sub>	0.05	0.10	0.15		AB	4.90	5.00	5.10	14
A <sub>2</sub>	0.85	0.90	0.95		AC	4.90	5.00	5.10	16
b	0.19	-	0.30	8	AD	6.40	6.50	6.60	20
b <sub>1</sub>	0.19	0.22	0.25		AE	7.70	7.80	7.90	24
c	0.090	-	0.20		AF	9.60	9.70	9.80	28
c <sub>1</sub>	0.090	0.127	0.135						
D	SEE VARIATIONS			4					
E	4.30	4.40	4.50	4					
e	0.65 BSC								
H	6.25	6.40	6.50						
L	0.50	0.60	0.70	5					
N	SEE VARIATIONS			6					
α	0°	4°	8°						

#### THIS TABLE IN INCHES

S V B O L	COMMON DIMENSIONS			N O T E	NOTE VARI- ATIONS	4 D			6 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A			.0433		AA	.114	.118	.122	8
A <sub>1</sub>	.002	.004	.006		AB	.193	.197	.201	14
A <sub>2</sub>	.0335	.0354	.0374		AC	.193	.197	.201	16
b	.0075	-	.0118	8	AD	.252	.256	.260	20
b <sub>1</sub>	.0075	.0087	.0098		AE	.303	.307	.311	24
c	.0035	-	.0079		AF	.378	.382	.386	28
c <sub>1</sub>	.0035	.0050	.0053						
D	SEE VARIATIONS			4					
E	.169	.173	.177	4					
e	.0256 BSC								
H	.246	.252	.256						
L	.020	.024	.028	5					
N	SEE VARIATIONS			6					
α	0°	4°	8°						

\*VARIATION AF IS DESIGNED BUT NOT TOOLED\*

