DENSE-PAC
MICROSYSTEMS

M-Densus
High Density Memory Device

8 Megabit
CMOS VIDEO RAM
DPO512X16MGY5-CM

PRELIMINARY

DESCRIPTION:

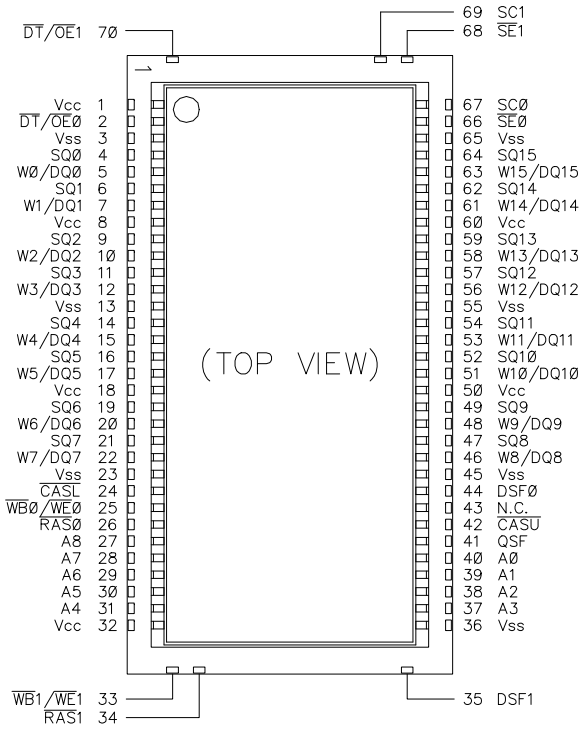
The DPO512X16MGY5-CM is a 512Kx16 bit Dual Port Dynamic RAM module that utilize the new and innovative space saving SOP stacking technology. The module is constructed of two Samsung© 256Kx16 CMOS Video RAMs each consists of 256Kx16 Dynamic Random Access Memory (RAM) port and 512Kx16 Static Serial Access Memory (SAM) port. The RAM and SAM port operate asynchronously except during data transfer between the ports.

The DPO512X16MGY5-CM provides for a compatible upgrade path to higher density compatible modules.

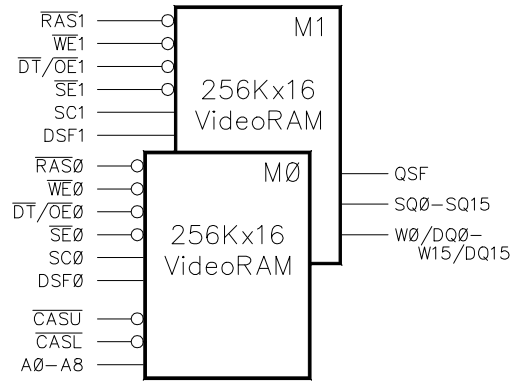
FEATURES:

- Access Times (DRAM/SAM):
  50/15, 60/15, 70/17ns (max.)
- Dual Port Video RAM
- Two 256Kx16 DRAM, 512Kx16 SAM with Individual Control
- Screened to -55°C to +125°C
- Single 5.0 ± 10% Supply Voltage, TTL Interface
- 512 Cycle/8ms Refresh
- Three Variations of Refresh:
  $\overline{CAS}$-Before-$\overline{RAS}$
  $\overline{RAS}$-Only
  Hidden Refresh
- Fast Page Mode with Extended Data Out
- RAM Read, Write, Read-Modify-Write
- Serial Read (SR)
- Split Read Transfer with Stop Operation (SRT)
- Read/Real Time Read Transfer (RT,RRT)
- Eight Column Block Write (BW) and Write per Bit with Masking Operation (New & Old Mask)
- Dual $\overline{CAS}$ Byte/Word Read/Write Operation
- Common Data Inputs and Outputs Using three state RAM Output Control
- All Inputs and Outputs TTL Compatible
- *M-Densus* Package:
  70-Pin Leadless Stack

PIN-OUT DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



PIN NAMES	
A0 - A8	Address inputs for the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 16 bit word out of the 262,144 available per device. Nine row address bits are latched on the falling edge of the row address strobe ($\overline{RAS}$) and the following nine column address bits are latched on the falling edge of the column address strobe.
W0/DQ0 - W15/DQ15	Data In / Data Out for DRAM access. These pins act as inputs for Mask and register load cycles, DQ Mask and Column Mask for BW.
SQ0 - SQ15	Serial output pin for serial read. (Serial write is not supported)
$\overline{CASL}$, $\overline{CASU}$	Column Address Strobes. $\overline{CASL}$, $\overline{CASU}$ are used to clock in the nine column address bits as a strobe forth DSF inputs and used to Byte/Word Read, Write Operations.
$\overline{RAS}$0, $\overline{RAS}$1	Row Address Strobe. $\overline{RAS}$ is used to clock the nine row bits for another input signal. The RAM port is placed in standby mode when the $\overline{RAS}$ control is held "High".
$\overline{WB}$0/$\overline{WE}$0, $\overline{WB}$1/$\overline{WE}$1	Data Write Enable. $\overline{WB}$/$\overline{WE}$ input is a multi-function pin. When $\overline{WB}$/$\overline{WE}$ is "High" at the falling edge of $\overline{RAS}$, during RAM port operation, it is used to write data into the memory array in the same as a standard DRAM. When $\overline{WB}$/$\overline{WE}$ is "Low" at the falling edge of $\overline{RAS}$, during RAM port operation, the W-P-B function is enabled.
$\overline{DT}$0/$\overline{OE}$0, $\overline{DT}$1/$\overline{OE}$1	The $\overline{DT}$/$\overline{OE}$ input is also a multi function pin. Enables and internal Transfer Operation at the falling edge of $\overline{RAS}$ when Transfer is enabled.
$\overline{SE}$0, $\overline{SE}$1	In serial read cycles , $\overline{SE}$ is used as an output control. When $\overline{SE}$ is "High", serial access is disabled, however, the serial address pointer is still incremented while SC is clocked.
SC0, SC1	Clock input to the serial address counter and data latch for the SAM register.
DSF0, DSF1	DSF is used to indicate which special functions (VW, FW, Split Transfer, etc.) are used for a particular access cycle.
QSF	QSF indicated which half of the SAM is being accessed. Low if address is 0 - 255, High if address is 256 - 511.
V_{CC}	Power Supply (+5.0V)
V_{SS}	Ground
N.C.	No Connect

RECOMMENDED OPERATING CONDITIONS					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Units**
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IL}	Input Low Voltage	-2.4	-	V_{CC}+1.0V	V
V_{IH}	Input High Voltage	-1.0	-	0.8	V

CAPACITANCE: V_{CC} = 5.0V, T_A = 25°C, f = 1MHz *				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
C_{IN1}	Input Capacitance: A0 - A8	4	12	pF
C_{IN2}	Input Capacitance: $\overline{CASU}$, $\overline{CASL}$, DSF	4	14	pF
C_{IN3}	Input Capacitance: SC, $\overline{SE}$, $\overline{DT}$/$\overline{OE}$, $\overline{RAS}$, $\overline{WB}$/$\overline{WE}$	2	7	pF
C_{DQ}	Input/Output Capacitance: W0/DQ0 - W15/DQ15	4	14	pF
C_{SQ}	Output Capacitance: SQ0 - SQ15, QSF	4	14	pf

* Values calculated not measured.

ABSOLUTE MAXIMUM RATINGS			
Symbol	**Parameter**	**Value**	**Units**
T_{STC}	Storage Temperature	-55 to +150	°C
V_{IN}	Input Voltage on Any Pin Relative to V_{SS}	-1.0 to +7.0	V
V_{OUT}	Output Voltage on Any Pin Relative to V_{SS}	-1.0 to +7.0	V
V_{CC}	V_{CC} Supply Voltage	-1.0 to +7.0	V
P_D	Power Dissipation	1	W
I_{OS}	Short Circuit Output Current	50	mA

NOTE: Permanent device damage may occur of "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of the component data sheet (Samsung KM4216C528). Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

INPUT/OUTPUT CURRENT: Recommended Operating Conditions unless otherwise specified					
Symbol	**Parameter**	**Conditions**	**Min.**	**Max.**	**Unit**
I_{IL}	Input Leakage Current	Any Input $0 \le V_{IN} \le V_{CC}$ +0.5V, All other pins not under test = 0 Volts	-20	+20	µA
I_{OL}	Output Leakage Current	Data out is disabled, $0 \le V_{OUT} \le V_{CC}$	-20	+20	µA
V_{OH}	Output High Voltage Level	RAM I_{OL} = -2mA, SAM I_{OL} = -2mA	2.4	-	V
V_{OL}	Output Low Voltage Level	RAM I_{OL} = 2mA, SAM I_{OL} = 2mA	-	0.4	V

DC OPERATING CHARACTERISTICS							
Symbol	**Characteristic** [1]	**RAM Port**	**SAM Port**	**50ns**	**60ns**	**70ns**	**Units**
I_{CC1}	Operating Current	$\overline{RAS}$ and $\overline{CAS}$ cycling @ t_{RC} = min.	Standby [2]	140	130	120	mA
I_{CC1} A			Active	180	170	155	
I_{CC2}	Standby Current	$\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ = V_{IH}, DSF = V_{IL}	Standby [2]	20	20	20	mA
I_{CC2} A			Active	65	60	55	
I_{CC3}	$\overline{RAS}$ - Only Refresh Current	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ Cycling @ t_{RC} = min.	Standby [2]	140	130	120	mA
I_{CC3} A			Active	180	170	155	
I_{CC4}	Extended Fast Page Mode Current	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling @ t_{RC} = min.	Standby [2]	140	130	120	mA
I_{CC4} A			Active	180	170	155	
I_{CC5}	$\overline{CAS}$ - Before - $\overline{RAS}$ Refresh Current	$\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC} = min.	Standby [2]	140	130	120	mA
I_{CC5} A			Active	180	170	155	
I_{CC6}	Data Transfer Current	$\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC} = min.	Standby [2]	170	150	140	mA
I_{CC6} A			Active	200	190	175	
I_{CC7}	Block Write Cycle Current	$\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC} = min.	Standby [2]	140	130	120	mA
I_{CC7} A			Active	180	170	155	
I_{CC8}	Color Register Load Current	$\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC} = min.	Standby [2]	130	120	100	mA
I_{CC8} A			Active	180	150	135	

1. Real values depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current. In I_{CC1}, I_{CC3}, I_{CC6}, I_{CC7}, I_{CC8}, address transition should be changed only once while $\overline{RAS}$ = V_{IL}. In I_{CC4}, address transition should be changed only once while $\overline{CAS}$ = V_{IH}.
2. SAM standby condition: $\overline{SE} \ge V_{IH}$, SC ≤ V_{IL} or ≥ V_{IH}.

PRELIMINARY

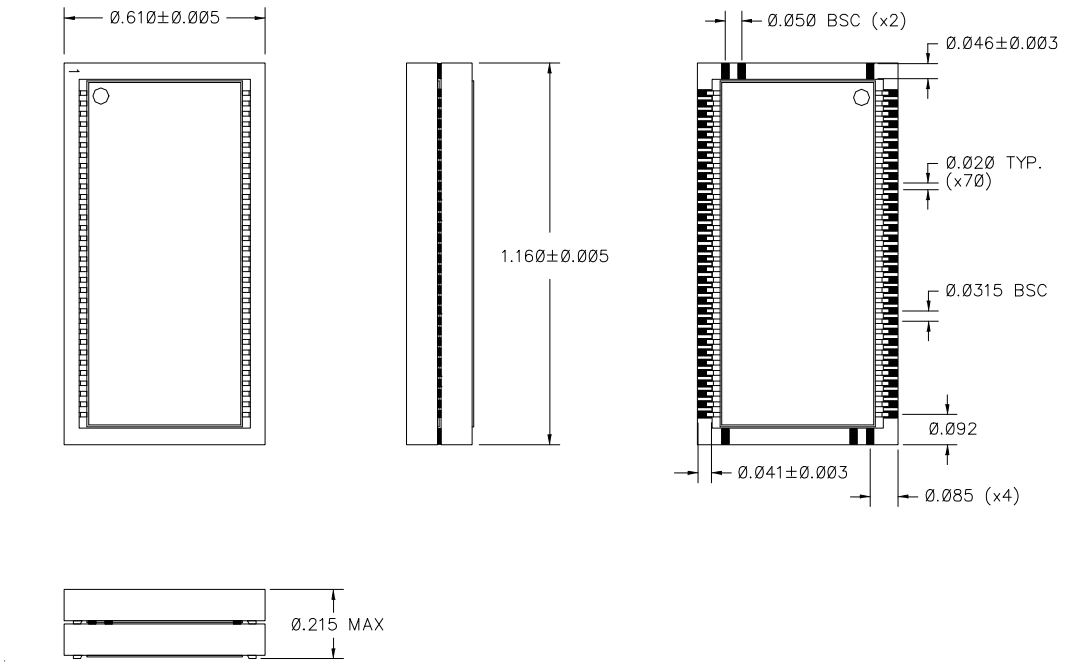
For additional operating, electrical and timing information see device manufacturers data sheet for Samsung part number KM4216C258 located at: http://www.usa.samsungsemi.com/products/prodspec/videoram/4216c258.pdf

ORDERING INFORMATION

DP	O	512	X	16	MG	Y5	– 5Ø	CM
PREFIX	TYPE	MEMORY DEPTH	DESIG	MEMORY WIDTH	DESIG	PACKAGE	SPEED	GRADE

- CM COMMERCIAL PROCESSED– MILITARY TEMPERATURE –55°C to +125°C
- 5Ø 50ns DRAM/15ns SAM
- 6Ø 60ns DRAM/15ns SAM
- 7Ø 70ns DRAM/17ns SAM
- TSOP STACK
- 4 MEGABIT SAMSUNG BASED DEVICES
- MEMORY MODULE WITHOUT SUPPORT LOGIC
- VIDIO RAM

MECHANICAL DRAWING



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