SGRAM 512K x 32 Bit x 2 Banks

Synchronous Graphic RAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Dual bank / Pulse $\overline{RAS}$
- MRS cycle with address key programs
  - CAS Latency (2, 3)
  - Burst Length (1, 2, 4, 8 & full page)
  - Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Burst Read Single-bit Write operation
- DQM 0-3 for byte masking
- Auto & self refresh
- 32ms refresh period (2K cycle)
- 100 pin QFP / TQFP

Graphic Features

- SMRS cycle
  - Load mask register
  - Load color register
- Write Per Bit (Old Mask)
- Block Write (8 Columns)

GENERAL DESCRIPTION

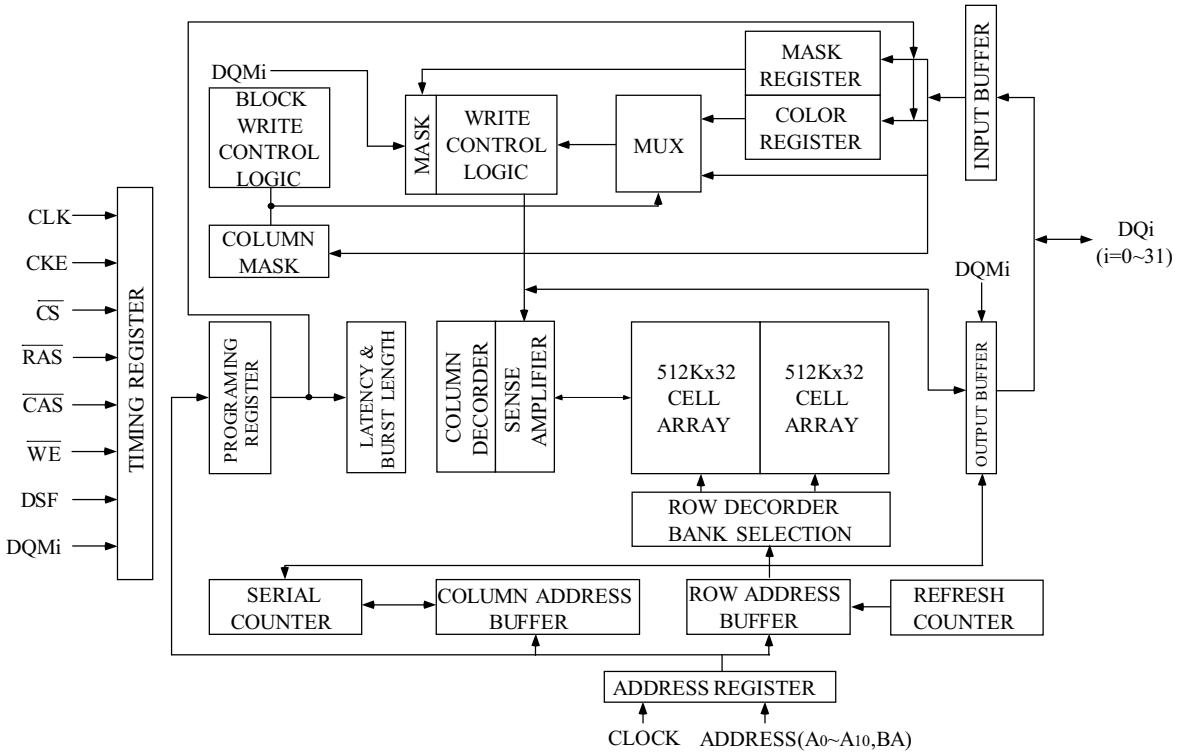
The M32L32321SA is 33, 554, 432 bits synchronous high data rate Dynamic RAM organized as 2 x 524, 288 words by 32 bits, fabricated with ESMT's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies , programmable burst length, and programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Write per bit and 8 columns block write improves performance in graphic systems.

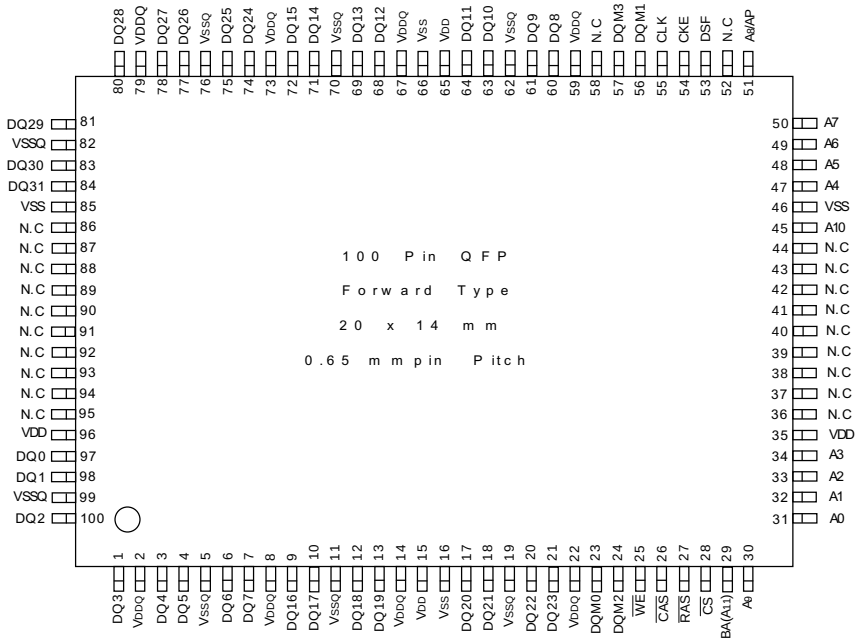
ORDERING INFORMATION

Part NO.	Cycle time	Clock Frequency	Access time@CL=3
M32L32321SA -5Q/-5F	5ns	200MHz	4.5ns
M32L32321SA -5.5Q/-5.5F	5.5ns	183MHz	5ns
M32L32321SA -6Q/-6F	6ns	166MHz	5.5ns
M32L32321SA -7Q/-7F	7ns	143MHz	6.0ns
M32L32321SA -8Q/-8F	8ns	125MHz	6.5ns

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



PIN DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	System Clock	Active on the positive going edge to sample all inputs
$\overline{CS}$	Chip Select	Disables or enable device operation by masking or enabling all inputs except CLK, CKE and DQMi
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one clock+ tss prior to new command. Disable input buffers for power down in standby.
A0 ~ A10	Address	Row / column addresses are multiplexed on the same pins. Row address : RA0~RA10, column address : CA0~CA7
BA	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank for read / write during column address latch time.
$\overline{RAS}$	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Column Address Strobe	Latches column address on the positive going edge of the CLK With $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Write Enable	Enables write operation and Row precharge.
DQMi	Data Input/Output Mask	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte Masking)
DQi	Data Input/Output	Data inputs/outputs are multiplexed on the same pins.
DSF	Define Special/ Function	Enables write per bit, block write and special mode register set.
V_{DD}/V_{SS}	Power Supply/ Ground	
V_{DDQ}/V_{SSQ}	Data Output Power/Ground	

ABSOLUTE MAXIMUM RATINGS (Voltage referenced to V_{SS})

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	
Input low voltage	V_{IL}	-0.3	0	0.8	V	Note 1
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-5	-	5	µA	Note 2
Output leakage current	I_{OL}	-5	-	5	µA	Note 3
Output Loading Condition	See Fig 1					

Note: 1. V_{IL}(min) = -1.5V AC (pulse width ≤ 5ns)
2. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DD}.

CAPACITANCE (V_{DD}/V_{DDQ} = 3.3V, T_A = 25 °C , f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11)	C_{IN1}	-	4	pF
Input capacitance (CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DSF& DQM0-3)	C_{IN2}	-	4	pF
Data input/output capacitance (DQ0 ~ DQ31)	C_{OUT}	-	5	pF

DECOUPLING CAPACITANCE GUIDE LINE

Recommended decoupling capacitance added to power line at board.

Parameter	Symbol	Value	Unit
Decoupling Capacitance between V_{DD} & V_{SS}	C_{DC1}	0.1+0.01	uF
Decoupling Capacitance between V_{DDQ} & V_{SSQ}	C_{DC2}	0.1+0.01	uF

***Note:** 1. V_{DD} and V_{DDQ} pins are separated each other.
All V_{DD} pins are connected in chip. All V_{DDQ} pins are connected in chip.
2. V_{SS} and V_{SSQ} pins are separated each other.
All V_{SS} pins are connected in chip. All V_{SSQ} pins are connected in chip.

DC CHARACTERISTICS

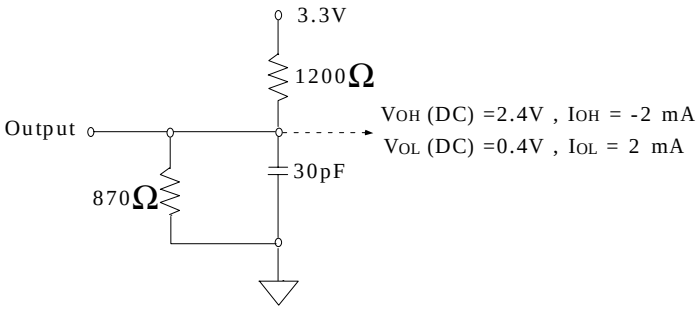
Recommended operating condition unless otherwise noted, T_A = 0 to 70 °C $V_{IH(min)}$ /$V_{IL(max)}$ =2.0V/0.8V

Parameter	Symbol	Test Condition	CAS Latency	Version -5	-5.5	-6	-7	-8	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length = 1 $t_{RC} \geq t_{RC(min)}$, $t_{CC} \geq t_{CC(min)}$ I_{OL} = 0 mA	3	230	210	190	160	140	mA	1
			2	230	210	190	160	140		
Precharge Standby Current in power-down mode	$I_{CC2}P$	CKE ≤ $V_{IL(max)}$, t_{CC} = 15ns		2	2	2	2	2	mA	
	$I_{CC2}PS$	CKE ≤ $V_{IL(max)}$, CLK ≤ $V_{IL(max)}$, t_{CC} = ∞		2	2	2	2	2		
Precharge Standby Current in non power-down mode	$I_{CC2}N$	CKE ≥ $V_{IH(min)}$, $\overline{CS}$ ≥ $V_{IH(min)}$, t_{CC} = 15ns Input signals are changed one time during 30ns		30	30	30	30	30	mA	
	$I_{CC2}NS$	CKE ≥ $V_{IH(min)}$, CLK ≤ $V_{IL(max)}$, t_{CC} = ∞ input signals are stable		2	2	2	2	2		
Active Standby Current in power-down mode	$I_{CC3}P$	CKE ≤ $V_{IL(max)}$, t_{CC} = 15ns		10	10	10	10	10	mA	
	$I_{CC3}PS$	CKE ≤ $V_{IL(min)}$, CLK ≤ $V_{IL(max)}$, t_{CC} = ∞		10	10	10	10	10		
Active Standby Current in non power-down mode (One Bank Active)	$I_{CC3}N$	CKE ≥ $V_{IH(min)}$, $\overline{CS}$ ≥ $V_{IH(min)}$, t_{CC} = 15ns Input signals are changed one time during 30ns		40	40	40	40	40	mA	
	$I_{CC3}NS$	CKE ≥ $V_{IH(min)}$, CLK ≤ $V_{IL(max)}$, t_{CC} = ∞ input signals are stable		10	10	10	10	10		
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA, Page Burst All Banks Activated, t_{CCD} = t_{CCD} (min)	3	250	230	210	180	160	mA	1, 2
			2	250	230	210	180	160		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC(min)}$	3	250	230	210	180	160	mA	3
			2	250	230	210	180	160		
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		1	1	1	1	1	mA	
Operating Current (One Bank Block Write)	I_{CC7}	$t_{CC} \geq t_{CC(min)}$, I_{OL} = 0 mA, $t_{BWC(min)}$		210	190	180	170	160	mA	4

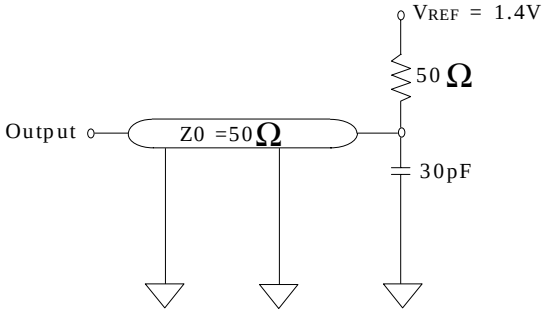
*Note : 1. Measured with outputs open.
2. Assumes minimum column address update cycle $t_{CCD(min)}$.
3. Refresh period is 32ms.
4. Assumes minimum column address update cycle $t_{BWC(min)}$.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value
AC Input levels	V_{IH}/V_{IL} = 2.4V/0.4V
Input timing measurement reference level	1.4V
Input rise and fall-time (See note3)	t_R/t_F = 1ns/1ns
Output timing measurement reference level	1.4V
Output load condition	See Fig. 2



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

AC CHARACTERISTICS

(AC operating conditions unless otherwise noted)

Parameter		Symbol	-5		-5.5		-6		-7		-8		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency =3	t_{CC}	5	1000	5.5	1000	6	1000	7	1000	8	1000	ns	1
	CAS latency =2		7		7		8		8.6		10			
CLK to valid output delay	CAS latency =3	t_{SAC}	-	4.5	-	5	-	5.5	-	6	-	6	ns	1, 2
	CAS latency =2		-	5	-	5.5	-	6	-	6	-	7		
Output data hold time	CAS latency =3	t_{OH}	2		2		2		2		2.5		ns	2
	CAS latency =2		2		2		2		2		2.5		ns	
CLK high pulse width		t_{CH}	2		2		2		2.5		3		ns	3
CLK low pulse width		t_{CL}	2		2		2		2.5		3		ns	3
Input setup time		t_{SS}	1.5		1.5		1.5		2		2.5		ns	3
Input hold time		t_{SH}	1		1		1		1		1		ns	3
CLK to output in Low-Z		t_{SLZ}	1		1		1		1		1		ns	2
CLK to output In Hi-Z	CAS latency =3	t_{SHZ}	-	4.5	-	5	-	5.5	-	6	-	6	ns	
	CAS latency =2		-	5	-	5.5	-	6	-	6	-	7		

* All AC parameters are measured from half to half.
*The 200MHz / 183MHz applications are guarantee only at Vcc 3.15V to 3.6V conditions.

*Note : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2 - 0.5) ns should be added to the parameter.
3. Assumed input rising and falling time (tr & tf) = 1ns.
If tr & tf is longer 1ns, transient time compensation should be considered.
i.e., [(tr + tf)/2 - 1] ns should be added to the parameter.

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version					Unit	Note
			-5	-5.5	-6	-7	-8		
Row active to row active delay		$t_{RRD(min)}$	10	11	12	14	16		1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	15	16	18	18	20	ns	1
Row precharge time		$t_{RP(min)}$	15	16	18	20	20	ns	1
Row active time		$t_{RAS(min)}$	38	38	42	42	48	ns	1
		$t_{RAS(max)}$	100					us	
Row cycle time		$t_{RC(min)}$	53	55	60	63	68	ns	1
Last data in to new col. address delay		$t_{CDL(min)}$	1					CLK	2
Last data in to row precharge		$t_{RDL(min)}$	1					CLK	2
Block write data-in to PRE command delay		$t_{BPL(min)}$	10	11	12	14	16	ns	
Block write data-in to Active (REF) command period (Auto precharge)		$t_{BAL(min)}$	25	27	30	35	40	ns	
Last data to burst stop		$t_{BDL(min)}$	5	6	6	7	8	ns	2
Col. Address to col. Address delay		$t_{CCD(min)}$	1					CLK	3
Block write cycle time		$t_{BWC(min)}$	2	2	2	2	2	CLK	4
Number of valid Output data	$\overline{CAS}$ latency = 3		2					CLK	5
	$\overline{CAS}$ latency = 2		1						

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change except block write cycle.
4. This parameter means minimum $\overline{CAS}$ to $\overline{CAS}$ delay at block write cycle only.
5. In case of row precharge interrupt, auto precharge and read burst stop.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

M32L32321SA-5Q/-5F (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		53ns	38ns	15ns	10ns	15ns	5ns	5ns	5ns
200 MHZ(5ns)	3	11	8	3	2	3	1	1	1
183 MHZ(5.5ns)	3	10	7	3	2	3	1	1	1
166 MHZ(6.0ns)	3	10	7	3	2	3	1	1	1
143 MHZ(7.0ns)	2	9	6	3	2	3	1	1	1
125 MHZ(8.0ns)	2	7	5	2	2	2	1	1	1
100 MHZ(10.0ns)	2	6	4	2	1	2	1	1	1

M32L32321SA-5.5Q/-5.5F (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		55ns	38ns	16ns	11ns	16ns	5.5ns	5.5ns	5.5ns
183 MHZ(5.5ns)	3	10	7	3	2	3	1	1	1
166 MHZ(6.0ns)	3	10	7	3	2	3	1	1	1
143 MHZ(7.0ns)	2	8	6	3	2	3	1	1	1
125 MHZ(8.0ns)	2	7	5	2	2	2	1	1	1
100 MHZ(10.0ns)	2	6	4	2	2	2	1	1	1
83 MHZ(12.0ns)	2	5	4	2	1	2	1	1	1

M32L32321SA-6Q/-6F (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		60ns	42ns	18ns	12ns	18ns	6ns	6ns	6ns
166 MHZ(6.0ns)	3	10	7	3	2	3	1	1	1
143 MHZ(7.0ns)	3	9	6	3	2	3	1	1	1
125 MHZ(8.0ns)	2	9	6	3	2	3	1	1	1
100 MHZ(10.0ns)	2	7	5	2	2	2	1	1	1
83 MHZ(12.0ns)	2	6	4	2	1	2	1	1	1
75 MHZ(13.4ns)	2	6	4	2	1	2	1	1	1

M32L32321SA-7Q/-7F (Unit : number of clock)

Frequency	CAS Latency	t_{RC} 63ns	t_{RAS} 42ns	t_{RP} 20ns	t_{RRD} 14ns	t_{RCD} 18ns	t_{CCD} 7ns	t_{CDL} 7ns	t_{RDL} 7ns
143 MHZ(7.0ns)	3	9	6	3	2	3	1	1	1
125 MHZ(8.0ns)	3	9	6	3	2	3	1	1	1
100 MHZ(10.0ns)	2	7	5	2	2	2	1	1	1
83 MHZ(12.0ns)	2	6	4	2	2	2	1	1	1
75 MHZ(13.4ns)	2	6	4	2	2	2	1	1	1
66 MHZ(15.0ns)	2	5	3	2	1	2	1	1	1

M32L32321SA -8Q/-8F (Unit : number of clock)

Frequency	CAS Latency	t_{RC} 68ns	t_{RAS} 48ns	t_{RP} 20ns	t_{RRD} 16ns	t_{RCD} 20ns	t_{CCD} 8ns	t_{CDL} 8ns	t_{RDL} 8ns
125 MHZ(8.0ns)	3	9	6	3	2	3	1	1	1
100 MHZ(10.0ns)	2	7	5	2	2	2	1	1	1
83 MHZ(12.0ns)	2	6	4	2	2	2	1	1	1
75 MHZ(13.4ns)	2	6	4	2	2	2	1	1	1
66 MHZ(15.0ns)	2	6	4	2	2	2	1	1	1
50 MHZ(20ns)	2	4	3	1	1	1	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	DQM	BA	A8	A0~A7,A9~A10	Note
Register	Mode Register set		H	X	L	L	L	L	L	X	OP CODE			1, 2
	Special Mode Register Set								H					1, 2, 7
Refresh	Auto Refresh		H	H	L	L	L	H	L	X	X			3
	Self Refresh	Entry		L										3
		Exit	L	H	L	H	H	H	X	X	X			3
					H	X	X	X						3
Bank Active & Row Addr.	Write Per Bit Disable		H	X	L	L	H	H	L	X	V	Row Address		4, 5
	Write Per Bit Enable								H					4,5,9
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	L	X	V	L	Column Address	4
	Auto Precharge Enable											H		4, 6
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	L	X	V	L	Column Address	4, 5
	Auto Precharge Enable											H		4,5,6,9
Block Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	H	X	V	L	Column Address	4, 5
	Auto Precharge Enable											H		4,5,6,9
Burst Stop			H	X	L	H	H	L	L	X	X			7
Precharge	Bank Selection		H	X	L	L	H	L	L	X	V	L	X	
	Both Banks										X	H		
Clock Suspend or Active Power Down		Entry	H	L	L	H	H	H	X	X	X			
					H	X	X	X						
		Exit	L	H	X	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	L	H	H	H	X	X	X			
					H	X	X	X						
		Exit	L	H	L	V	V	V	V	X				
					H	X	X	X	X					
DQM			H	X						V	X			8
No Operation Command			H	X	L	H	H	H	X	X	X			
					H	X	X	X						

(V = Valid, X = Don't Care. H = Logic High, L = Logic Low)

Note : 1.OP Code : Operand Code
A0~A10,BA : Program keys. (@ MRS)
A5, A6 : LMR & LCR select. (@ SMRS)
Color register exists only one per DQi which both banks share.
So does Mask Register.
Color or mask is loaded into chip through DQ pin.
2.MRS can be issued only at both banks precharge state.
SMRS can be issued only if DQ's are idle.
A new command can be issued at the next clock of MRS/SMRS.

3.Auto refresh functions as same as CBR refresh of DRAM.
The automatical precharge without Row precharge of command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.
4.BA : Bank select address.
If "Low" at read, (block) write, Row active and precharge, bank A is selected.
If "High" at read, (block) write, Row active and precharge, bank B is selected.
If A8 is "High" at Row precharge, BA is ignored and both banks are selected.
5.It is determined at Row active cycle.
whether Normal/Block write operates in write per bit mode or not.
For A bank write, at A bank Row active, for B bank write, at B bank Row active.
Terminology : Write per bit = I/O mask
(Block) Write with write per bit mode = Masked (Block) Write
6.During burst read or write with auto precharge, new read/(block) write command cannot be issued.
Another bank read/(block) write command can be issued at t_{RP} after the end of burst.
7.Burst stop command is valid for all burst length.
8.DQM sampled at positive going edge of a CLK.
masks the data-in at the very CLK (Write DQM latency is 0)
but makes Hi-Z state the data-out of 2 CLK cycles after.(Read DQM latency is 2)
9.Graphic features added to SDRAM's original features.
If DSF is tied to low, graphic functions are disabled and chip operates as a 32M SDRAM with 32 DQ's.

SGRAM vs SDRAM

SDRAM Function	MRS		Bank Active		Write	
DSF	L	H	L	H	L	H
SGRAM Function	MRS	SMRS	Bank Active With Write per bit Disable	Bank Active With Write per bit Enable	Normal Write	Block Write

If DSF is low. SGRAM functionality is identical to SDRAM functionality.

SGRAM can be uesed as an unified memory by the appropriate DSF control
→ SGRAM = Graphic Memory + Main Memory.

MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with MRS

Address	BA	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	RFU	RFU	W.B.L	TM		CAS Latency			BT	Burst Length		
	(Note1)		(Note2)									

Test Mode			CAS Latency				Burst Type		Burst Length				
A8	A7	Type	A6	A5	A4	Latency	A3	Type	A2	A1	A0	BT = 0	BT = 1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential	0	0	0	1	Reserved
0	1	Vendor	0	0	1	-	1	Interleave	0	0	1	2	Reserved
1	0	Use	0	1	0	2			0	1	0	4	4
1	1	Only	0	1	1	3			0	1	1	8	8
Write Burst Length			1	0	0	Reserved			1	0	0	Reserved	Reserved
A9	Length		1	0	1	Reserved			1	0	1	Reserved	Reserved
0	Burst		1	1	0	Reserved			1	1	0	Reserved	Reserved
1	Single Bit		1	1	1	Reserved			1	1	1	256(Full)	Reserved

(Note 3)

Special Mode Register Programmed with SMRS

Address	BA	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	X					LC	LM	X				

Load Color		Load Mask	
A6	Function	A5	Function
0	Disable	0	Disable
1	Enable	1	Enable

(Note 4)

POWER UP SEQUENCE

1.Apply power and start clock, Attempt to maintain CKE = ”H”, DQM = ”H” and the other pin are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200μs.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.
cf.) Sequence of 4 & 5 may be changed.

The device is now ready for normal operation.

Note : 1. RFU(Reserved for Future Use) should stay “0” during MRS cycle.
2. If A9 is high during MRS cycle, “Burst Read Single Bit Write” function will be enabled.
3. The full column burst (256bit) is available only at Sequential mode of burst type.
4. If LC and LM both high (1), data of mask and color register will be unknown.

BURST SEQUENCE (BURST LENGTH = 4)

Initial Address		Sequential				Interleave			
A1	A0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

BURST SEQUENCE (BURST LENGTH = 8)

Initial address			Sequential								Interleave							
A2	A1	A0																
0	**0**	**0**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
0	**0**	**1**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**0**	**1**	**0**	**3**	**2**	**5**	**4**	**7**	**6**
0	**1**	**0**	**2**	**3**	**4**	**5**	**6**	**7**	**0**	**1**	**2**	**3**	**0**	**1**	**6**	**7**	**4**	**5**
0	**1**	**1**	**3**	**4**	**5**	**6**	**7**	**0**	**1**	**2**	**3**	**2**	**1**	**0**	**7**	**6**	**5**	**4**
1	**0**	**0**	**4**	**5**	**6**	**7**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**0**	**1**	**2**	**3**
1	**0**	**1**	**5**	**6**	**7**	**0**	**1**	**2**	**3**	**4**	**5**	**4**	**7**	**6**	**1**	**0**	**3**	**2**
1	**1**	**0**	**6**	**7**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**4**	**5**	**2**	**3**	**0**	**1**
1	**1**	**1**	**7**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

PIXEL to DQ MAPPING (at BLOCK WRITE)

Column address			3 Byte	2 Byte	1 Byte	0 Byte
A2	A1	A0	I/O31~ I/O24	I/O23~ I/O16	I/O15~ I/O8	I/O7~ I/O0
0	0	0	DQ24	DQ16	DQ8	DQ0
0	0	1	DQ25	DQ17	DQ9	DQ1
0	1	0	DQ26	DQ18	DQ10	DQ2
0	1	1	DQ27	DQ19	DQ11	DQ3
1	0	0	DQ28	DQ20	DQ12	DQ4
1	0	1	DQ29	DQ21	DQ13	DQ5
1	1	0	DQ30	DQ22	DQ14	DQ6
1	1	1	DQ31	DQ23	DQ15	DQ7

DEVICE OPERATIONS

CLOCK (CLK)

The clock input is used as the reference for all SGRAM operations. All operations are synchronized to the positive going edge of the clock. The clock transitions must be monotonic between V_{IL} and V_{IH}. During operation with CKE high all inputs are assumed to be in valid state (low or high) for the duration of setup and hold time around positive edge of the clock for proper functionality and Icc specifications.

CLOCK ENABLE(CKE)

The clock enable (CKE) gates the clock onto SGRAM. If CKE goes low synchronously with clock (set-up and hold time same as other inputs), the internal clock suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. All other inputs are ignored from the next clock cycle after CKE goes low. When both banks are in the idle state and CKE goes low synchronously with clock, the SGRAM enters the power down mode from the next clock cycle. The SGRAM remains in the power down mode ignoring the other inputs as long as CKE remains low. The power down exit is synchronous as the internal clock is suspended. When CKE goes high at least "tss+1CLOCK" before the high going edge of the clock, then the SGRAM becomes active from the same clock edge accepting all the input commands.

BANK SELECT (BA)

This SGRAM is organized as two independent banks of 524, 288 words x 32 bits memory arrays. The BA inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. When BA is asserted low, bank A is selected. When BA is latched high, bank B is selected. The banks select BA is latched at bank activate, read, write, mode register set and precharge operations.

ADDRESS INPUTS (A0~A10)

The 19 address bits are required to decode the 524,288 word locations are multiplexed into 10 address input pins (A0~A10). The 11 bit row address is latched along with $\overline{RAS}$ and BA during bank activate command. The 8 bit column address is latched along with $\overline{CAS}$, $\overline{WE}$ and BA during read or with command.

NOP and DEVICE DESELECT

When $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high, The SGRAM performs no operation (NOP). NOP does not initiate any new operation, but is needed to complete operations which require more than single clock cycle like bank activate, burst read, auto refresh, etc. The device deselect is also a NOP and is entered by asserting $\overline{CS}$ high. $\overline{CS}$ high disables the command decoder so that $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DSF and all the address inputs are ignored.

POWER-UP

The following sequence is recommended for POWER UP

1. Power must be applied to either CKE and DQM inputs to pull them high and other pins are NOP condition at the condition at the inputs before or along with V_{DD} (and V_{DDQ}) supply.
   The clock signal must also be asserted at the same time.
2. After V_{DD} reaches the desired voltage, a minimum pause of 200 microseconds is required with inputs in NOP condition.
3. Both banks must be precharged now.
4. Perform a minimum of 2 Auto refresh cycles to stabilize the internal circuitry.
5. Perform a MODE REGISTER SET cycle to program the CAS latency, burst length and

DEVICE OPERATIONS (Continued)

burst type as the default value of mode register is undefined.
At the end of one clock cycle from the mode register set cycle, the device is ready for operation.
When the above sequence is used for Power-up, all the outputs will be in high impedance state. The high impedance of outputs is not guaranteed in any other power-up sequence.
cf.) Sequence of 4 & 5 may be changed.

MODE REGISTER SET (MRS)

The mode register stores the data for controlling the various operating modes of SGRAM. It programs the CAS latency, burst type, addressing, burst length, test mode and various vendor specific options to make SGRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SGRAM. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and DSF (The SGRAM should be in active mode with CKE already high prior to writing the mode register). The state of address pins A0~A10 and BA in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and DSF going low is the data written in the mode register. One clock cycles is required to complete the write in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as both banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length field uses A0~A2, burst type uses A3, CAS latency (read latency from column address) A4~A6, A7~A8 ,A10 and BA are uses for vendor specific options or test mode use. And the write burst length is programmed using A9. A7~A8, A10 and BA must be set to low for normal SGRAM operation. Refer to the table for specific codes for various burst length, addressing modes and $\overline{CAS}$ latencies.

BANK ACTIVATE

The bank activate command is used to select a random row in an idle bank. By asserting low on $\overline{RAS}$ and $\overline{CS}$ with desired row and bank addresses, a row access is initiated. The read or write operation can occur after a time delay of $t_{RCD\ (min)}$ from the time of bank activation. $t_{RCD\ (min)}$ is the internal timing parameter of SGRAM, therefore it is dependent on operating clock frequency. The minimum number of clock cycles required between bank activate and read or write command should be calculated by dividing $t_{RCD\ (min)}$ with cycle time of the clock and then rounding of the result to the next higher integer. The SGRAM has two internal banks in the same chip and shares part of the internal circuitry to reduce chip area, therefore it restricts the activation of both banks immediately. Also the noise generated during sensing of each bank of SGRAM is high requiring some time for power supplies to recover before another bank can be sensed reliably. $t_{RRD\ (min)}$ specifies the minimum time required between activating different bank. The number of clock cycles required between different bank activation must be calculated similar to t_{RCD} specification. The minimum time required for the bank to be active to initiate sensing and restoring the complete row of dynamic cells is determined by $t_{RAS\ (min)}$. Every SGRAM bank activate command must satisfy $t_{RAS\ (min)}$ specification before a precharge command to that active bank can be asserted. The maximum time any bank can be in the active state is determined by t_{RAS} (max). The number of cycles for both $t_{RAS(min)}$ and t_{RAS} (max) can be calculated similar to t_{RCD} specification.

BURST READ

The burst read command is used to access burst of data on consecutive clock cycles from an

DEVICE OPERATIONS (Continued)

active row in an active bank. The burst read command is issued by asserting low on $\overline{CS}$ and $\overline{RAS}$ with $\overline{WE}$ being high on the positive edge of the clock. The bank must be active for at least $t_{RCD\ (min)}$ before the burst read command is issued. The first output appears in $\overline{CAS}$ latency number of clock cycles after the issue of burst read command. The burst length, burst sequence and latency from the burst read command is determined by the mode register which is already programmed. The burst read can be initiated on any column address of the active row. The address wraps around if the initial address does not start from a boundary such that number of outputs from each I/O are equal to the burst length programmed in the mode register. The output goes into high-impedance at the end of burst, unless a new burst read was initiated to keep the data output gapless. The burst read can be terminated by issuing another burst read or burst write in the same bank or the other active bank or a precharge command to the same bank. The burst stop command is valid for all burst length.

BURST WRITE

The burst write command is similar to burst read command, and is used to write data into the SGRAM on consecutive clock cycles in adjacent addresses depending on burst length and burst sequence. By asserting low on $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ with valid column address, a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even though the internal writing may not have been completed yet. The writing can not complete burst length. The burst write can be terminated by issuing a burst read and DQM for blocking data inputs or burst write in the same or the other active bank.

The write burst can also be terminated by using DQM for blocking data and precharging the bank "t_{RDL}" after the last data input to be written into the active row. See DQM OPERATION also.

DQM OPERATION

The DQM is used mask input and output operations. It works similar to $\overline{OE}$ during operation and inhibits writing during write operation. The read latency is two cycles from DQM and zero cycle for write, which means DQM masking occurs two cycles later in read cycle and occurs in the same cycle during write cycle. DQM operation is synchronous with the clock. The DQM signal is important during burst interrupts of write with read or precharge in the SGRAM. Due to asynchronous nature of the internal write, the DQM operation is critical to avoid unwanted or incomplete writes when the complete burst write is required. DQM is also used for device selection and bus control in a memory system. DQM0 controls DQ0 to DQ7, DQM1 controls DQ8 to DQ15, DQM2 controls DQ16 to DQ23, DQM3 controls DQ24 to DQ31. DQM masks the DQ's by a byte regardless that the corresponding DQ's are in a state of WPB masking or Pixel masking. Please refer to DQM timing diagram also.

PRECHARGE

The precharge is performed on an active bank by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ and A8/AP with valid BA of the bank to be precharged. The precharge command can be asserted anytime after $t_{RAS\ (min)}$ is satisfy from the bank activate command in the desired bank. "t_{RP}" is defined as the minimum time required to precharge a bank.

DEVICE OPERATIONS (Continued)

The minimum number of clock cycles required to complete row precharge is calculated by dividing "t_{RP}" with clock cycle time and rounding up to the next higher integer. Care should be taken to make sure that burst write is completed or DQM is used to inhibit writing before precharge command is asserted. The maximum time any bank can be active is specified by t_{RAS} (max). Therefore, each bank has to be precharged within t_{RAS} (max) from the bank activate command. At the end of precharge, the bank enters the idle state and is ready to be activated again.
Entry to Power Down, Auto refresh, Self refresh and Mode register Set etc. is possible only when both banks are in idle state.

AUTO PRECHARGE

The precharge operation can also be performed by using auto precharge. The SGRAM internally generates the timing to satisfy $t_{RAS\ (min)}$ and "t_{RP}" for the programmed burst length and $\overline{CAS}$ latency. The auto precharge command is issued at the same time as burst write by asserting high on A8/AP. If burst read or burst write command is issued with low on A8/AP, the bank is left active until a new command is asserted. Once auto precharge command is given, no new command are possible to that particular bank until the bank achieves idle state.

BOTH BANKS PRECHARGE

Both banks can be precharged at the same time by using Precharge all command. Asserting low on $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ with high on A8/AP after all banks have satisfied $t_{RAS\ (min)}$ requirement, performs precharge on both banks. At the end of t_{RP} after performing precharge all, all banks are in idle state.

AUTO REFRESH

The storage cells of SGRAM need to be refreshed every 32ms to maintain data. An auto refresh cycle accomplishes refresh of a single row of storage cells. The internal counter increments automatically on every auto refresh cycle to refresh all the rows. An auto refresh command is issued by asserting low on $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ with high on CKE and $\overline{WE}$. The auto refresh command can only be asserted with both banks being in idle state and the device is not in power down mode (CKE is high in the previous cycle). The time required to complete the auto refresh operation is specified by $t_{RC\ (min)}$. The minimum number of clock cycles required can be calculated by driving t_{RC} with clock cycle time and them rounding up to the next higher integer. The auto refresh command must be followed by NOP's until the auto refresh operation is completed. Both banks will be in the idle state at the end of auto refresh operation. The auto refresh is the preferred refresh mode when the SGRAM is being used for normal data transactions. The auto refresh cycle can be performed once in 15.6us or the burst of 2048 auto refresh cycles in 32ms.

SELF REFRESH

The self refresh is another refresh mode available in the SGRAM. The self refresh is the preferred refresh mode for data retention and low power operation of SGRAM. In self refresh mode, the SGRAM disables the internal clock and all the input buffers except CKE. The refresh addressing and timing is internally generated to reduce power consumption.
The self refresh mode is entered from all banks idle state by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE with high on $\overline{WE}$. Once the self refresh mode is entered, only CKE state

DEVICE OPERATIONS (Continued)

being low matters, all the other inputs including clock are ignored to remain in the refresh.
The self refresh is exited by restarting the external clock and then asserting high on CKE. This must be followed by NOP's for a minimum time of t_{RC} before the SGRAM reaches idle state to begin normal operation. If the system uses burst auto refresh during normal operation, it is recommended to use burst 2048 auto refresh cycles immediately after exiting self refresh.

DEFINE SPECIAL FUNCTION(DSF)

The DSF controls the graphic applications of SGRAM. If DSF is tied to low, SGRAM functions as 512K x 32 x 2 Bank SDRAM. SGRAM can be used as an unified memory by the appropriate DSF command. All the graphic function mode can be entered only by setting DSF high when issuing commands which otherwise would be normal SDRAM commands.

SDRAM functions such as $\overline{RAS}$ Active, Write and WCBR change to SGRAM functions such as $\overline{RAS}$ Active with WPB, Block Write and SWCBR respectively that DSF controls.

SPECIAL MODE REGISTER SET(SMRS)

There are two kinds of special mode registers in SGRAM. One is color register and the other is mask register. Those usage will be explained at "WRITE PER BIT" and "BLOCK WRITE" session. When A5 and DSF goes high in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low, load color register is filled with color data for associated DQ's through the DQ pins. If both A5 and A6 are high at SMRS, data of mask and color cycle is required to complete the write in the mask register and the color register at LMR and LCR respectively. The next color of LMR and LCR, a new commands can be issued. SMRS, compared with MRS, can be issued at the active state under the condition that DQ's are idle. As in write operation, SMRS accepts the data needed through DQ pins. Therefore it should be attended not to induce bus contention. The more detailed materials can be obtained by referring corresponding timing diagram.

WRITE PER BIT

Write per bit(i.e. I/O mask mode) for SGRAM is a function that selectively masks bits of data being written to the devices. The mask is stored in an internal register and applied to each bit of data written when enable. Bank active command with DSF=High enable write per bit for the associated bank. The mask used for write per bit operations is stored in the mask register accessed by SWCBR (Special Mode Register Set Command). When a mask bit=0, the associated data bit is unaltered when a write command is executed and the write per bit has been enable for the bank being written. No additional timing conditions. Write per bit writes can be either masking is the same for write per bit and non-WPB write.

BLOCK WRITE

Block write is a feature allowing the simultaneous writing of consecutive 8 columns of data within a RAM device during a single access cycle. During block write the data to be written comes from the internal "color" register and DQ I/O pins are used for independent column selection. The block of column to be written is aligned on 8 column boundaries and is defined by the column address with the 3 LSB's ignored. Write command with DSF=1 enable block write for the associated bank. The block width is 8 column where column ="n" bits for by "n" part. The color register is the same width as the data port of the chip. It is width via a SWCBR where data present on the DQ pins is

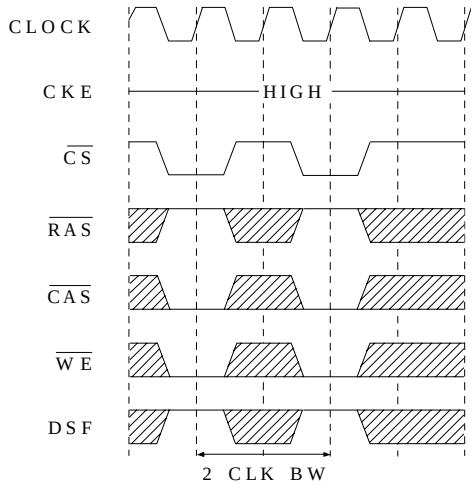
DEVICE OPERATIONS (Continued)

to be coupled into the internal color register. The color register provides the data masked by the DQ column select, WPB mask (if enable), and DQM byte mask. Column data masking (Pixel masking) is provided on an individual column basis for each byte of data. The column mask is driven on the DQ pins during a block write command. The DQ column mask function is segmented on a per bit basis (i.e. DQ [0:7] provided the column mask for data bits [0:7], DQ [8:15] provided the column mask for data bits [8:15], DQ0 masks column [0] for data bits[0:7], DQ9 masks column [1] for data bits[8:15], etc). Block writes are always non-burst independent of the burst length that has been programmed into to the mode register. If write per bit was enabled by the bank active command with DSF=1, then write per bit masking of the color register data is enabled.

If write per bit was disabled by a bank active command with DSF=0, the write per bit masking of the color register data is disabled. DQM masking provides independent data byte masking during normal write operations, except that the control is extended to the consecutive 8 columns of the block write.

Timing Diagram to Illustrate t_{BWC}

1. 2CLK Cycle Block Write

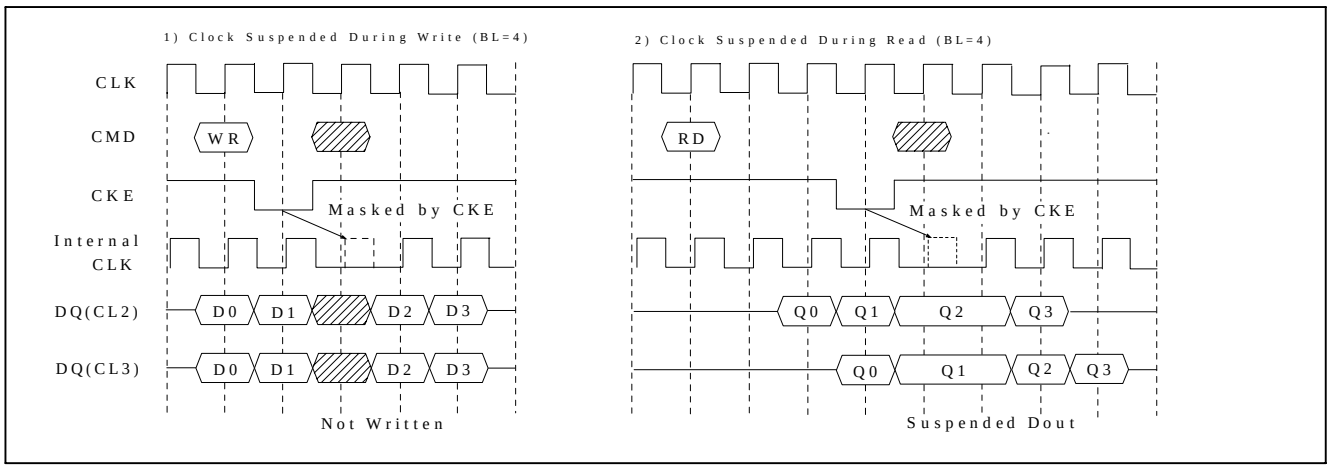


SUMMARY OF 2M Byte SGRAM BASIC FEATURES AND BENEFITS

Features	256K x 32 x 2 SGRAM	Benefits
Interface	Synchronous	Better interaction between memory and system without wait-state of asynchronous DRAM. High speed vertical and horizontal drawing. High operation frequency allows performance gain for SCROLL, FILL, and BitBLT.
Bank	2ea	Pseudo-infinite row length by on-chip interleaving operation. Hidden row activation precharge.
Page Depth /1 Row	256 bit	High speed vertical and horizontal drawing.
Total Page Depth	2048 bytes	High speed vertical and horizontal drawing.
Burst length (Read)	1, 2, 4, 8 Full Page	Programmable burst of 1, 2, 4, 8 and full page transfer per column address.
Burst length (Write)	1, 2, 4, 8 Full Page	Programmable burst of 1, 2, 4, 8 and full page transfer per column address.
	BRSW	Switch to burst length of 1 at write without MRS.
Burst Type	Sequential & Interleave	Compatible with Intel and Motorola CPU based system.
CAS Latency	2, 3	Programmable CAS latency.
Block Write	8 Column	High speed FILL, CLEAR, Text with color registers. Maximum 32 byte data transfer (e.g. for 8bpp : 32 pixels) with plane and byte masking functions.
Color Register	1ea.	A and B bank share.
Mask Register	1 ea.	Write-per-bit capability (bit plane masking). A and B bank share.
	DQM0~3	Byte masking (pixel masking for 8bpp system) for data-out/in
Mask function	Write per bit	Each bit of the mask register directly controls a corresponding bit plane.
	Pixel Mask at Block Write	Byte masking (pixel masking for 8bpp system) for color DQi.

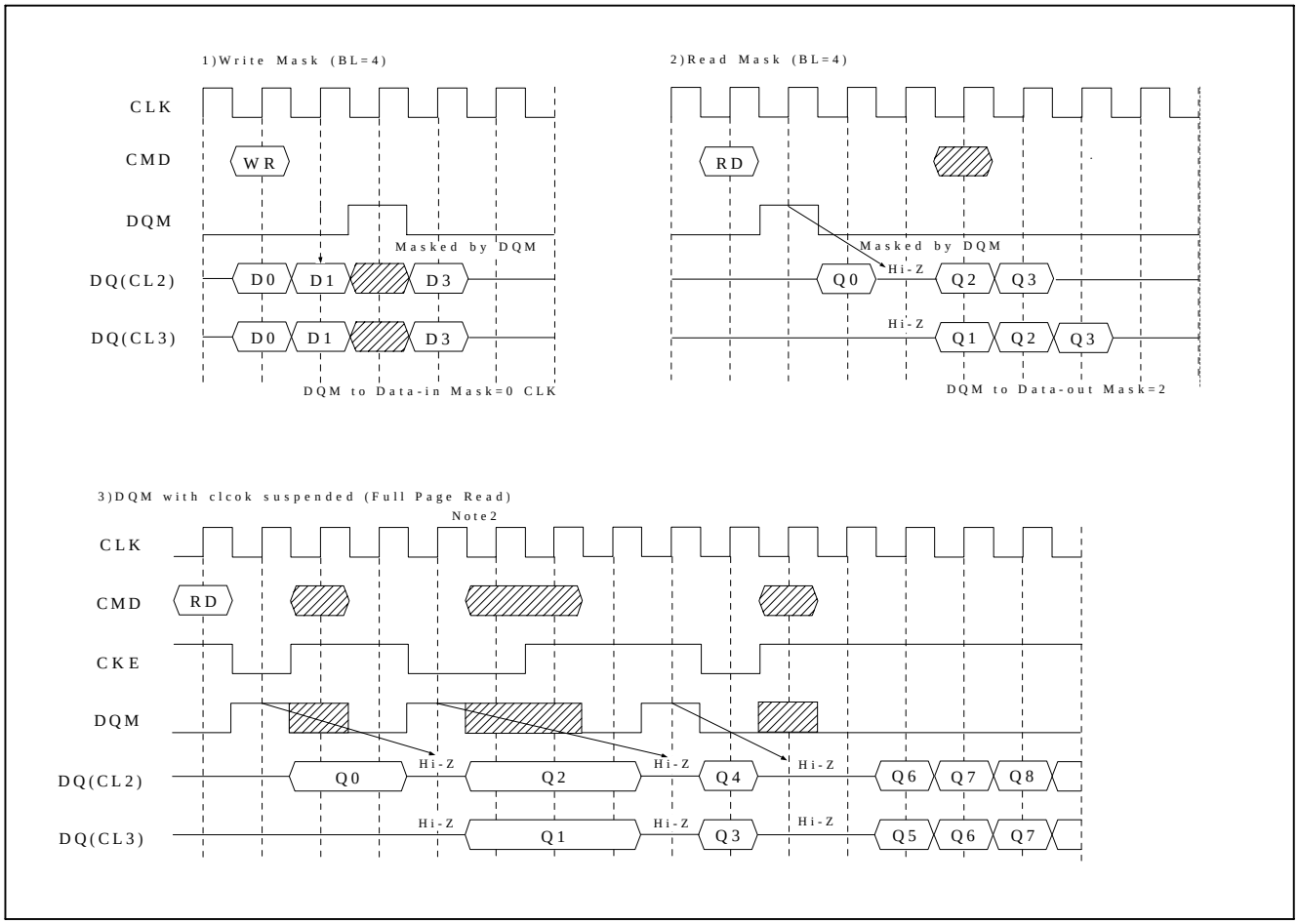
BASIC FEATURE AND FUNCTION DESCRIPTION

1.CLOCK Suspend



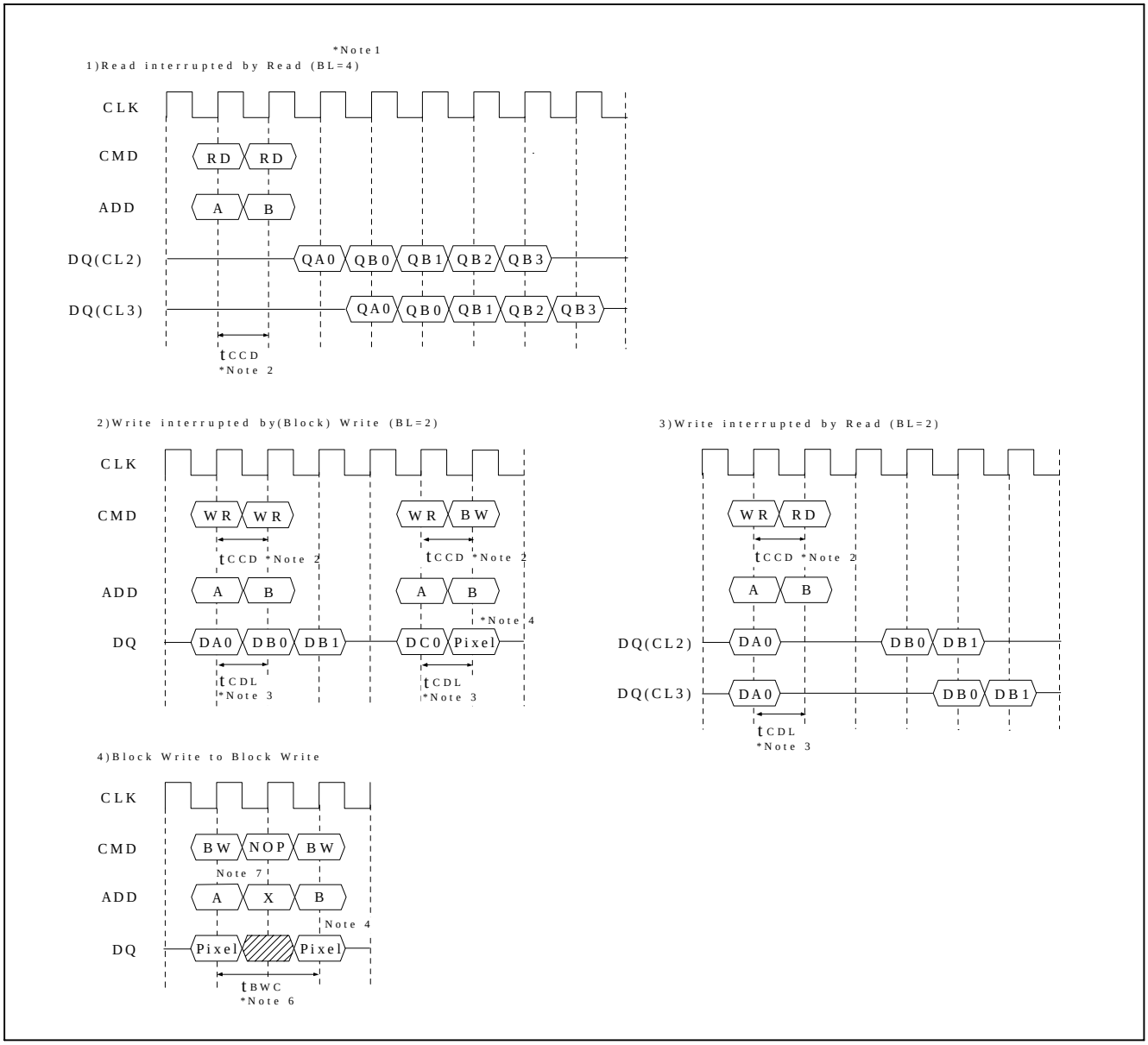
*Note : CKE to CLK disable/enable=1 clock

2. DQM Operation



*Note : 1. There are 4 DQMi (i = 0~3).
Each DQMi masks 8 DQ's. (1 Byte, 1 Pixel for 8bpp).
2. DQM masks data out Hi-Z after 2 clocks which should masked by CKE "L".

3. $\overline{CAS}$ Interrupt (I)



*Note : 1. By "Interrupt", It is possible to stop burst read/write by external before the end of burst.

By "$\overline{CAS}$ Interrupt", to stop burst read/write by $\overline{CAS}$ access ; read, write and block write.

2.t_{CCD} : $\overline{CAS}$ to $\overline{CAS}$ delay.(=1CLK)

3.t_{CDL} : Last Data in to new column address delay.(=1CLK)

4.Pixel : Pixel mask.

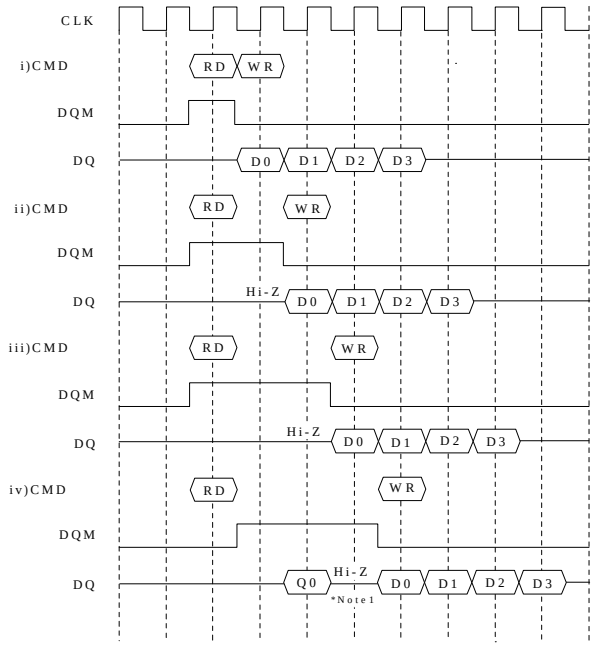
5.t_{CC} : Clock cycle time.

6.t_{BWC} : Block write minimum cycle time.

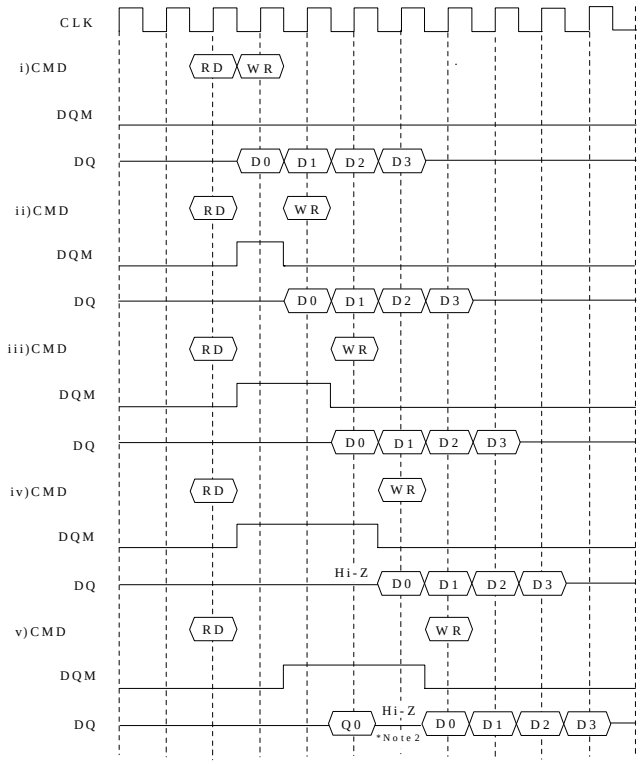
7.Other Bank can be active or precharge.

4. $\overline{\text{CAS}}$ Interrupt (II) : Read Interrupted by Write & DQM

(1) CL=2, BL=4

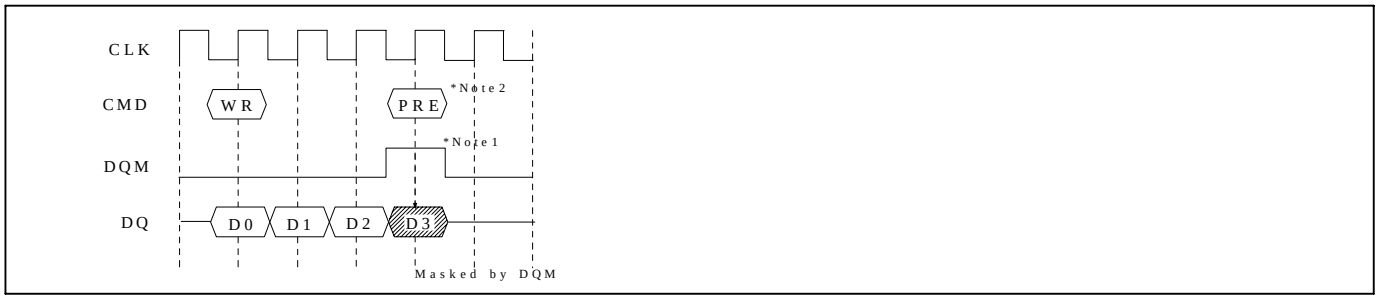


(2) CL=3 , BL=4



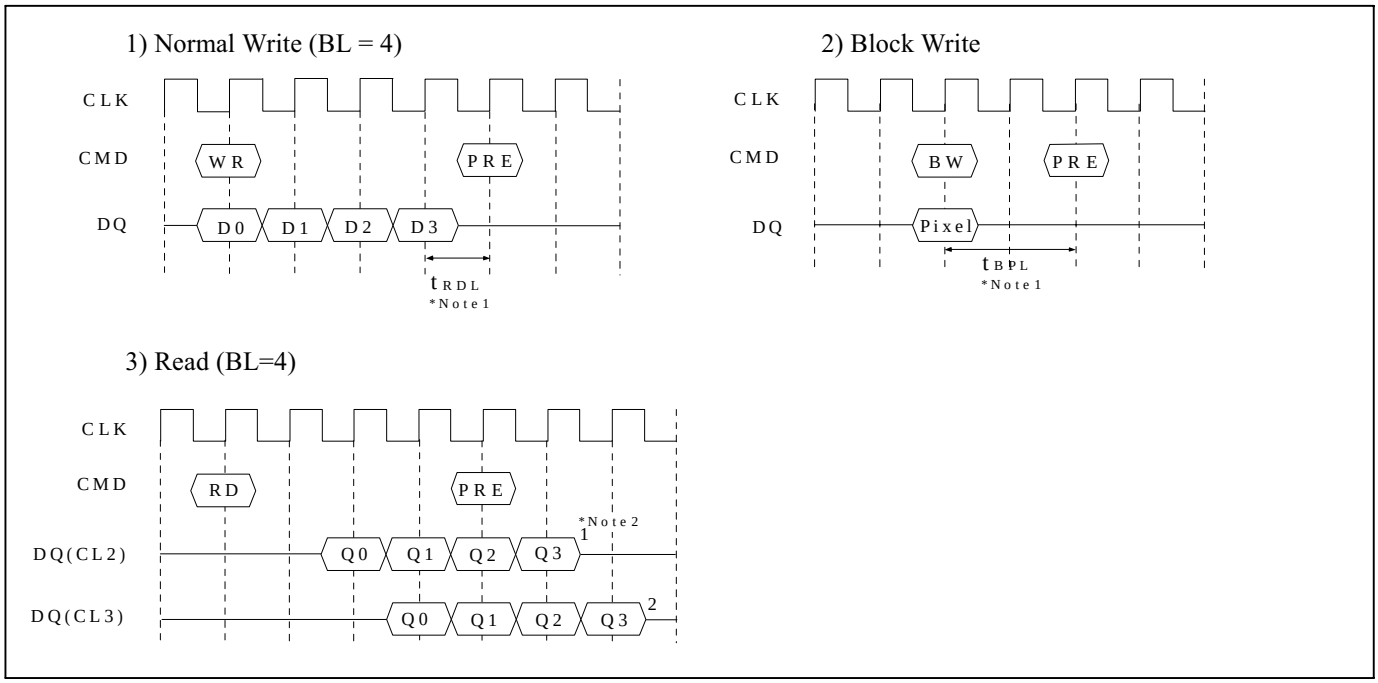
*Note : 1. To prevent bus contention, there should be at least one gap between data in and data out.
2. To prevent bus contention, DQM should be issued which makes at least one gap between data in and data out.

5. Write Interrupted by Precharge & DQM

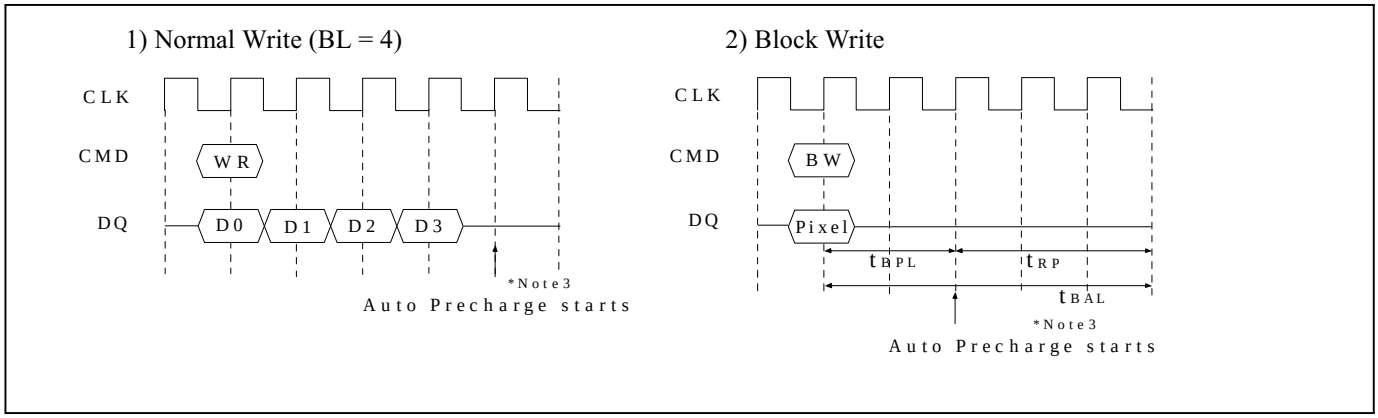


*Note : 1. To inhibit invalid write, DQM should be issued.
2. This precharge command and burst write command should be of the same bank, otherwise it is not precharge interrupt but only another bank precharge of dual banks operation.

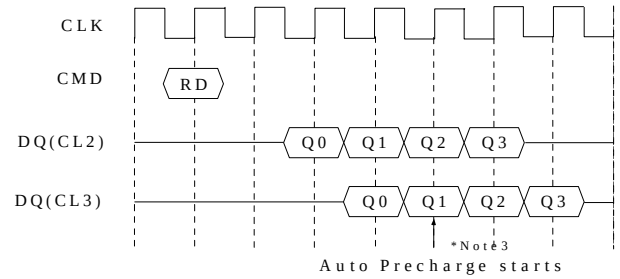
6. Precharge



7. Auto Precharge



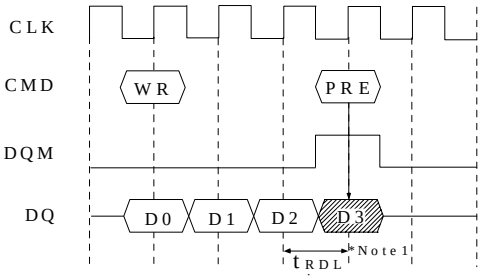
3) Read (BL=4)



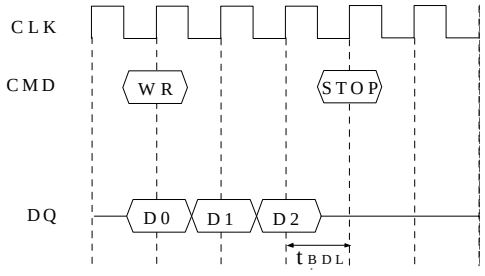
*Note : 1. t_{RDL} : Write data-in to PRE command delay, t_{BPL} : Block Write data-in to PRE command delay.
2. Number of valid output data after row precharge : 1, 2 for CAS Latency = 2, 3 respectively.
3. The row active command of the precharge bank can be issued after t_{RP} from this point.
The new read/write command of other activated bank can be issued from this point.
At burst read/write with auto precharge, $\overline{CAS}$ interrupt of the same bank is illegal.

8. Burst Stop & Precharge Interrupted

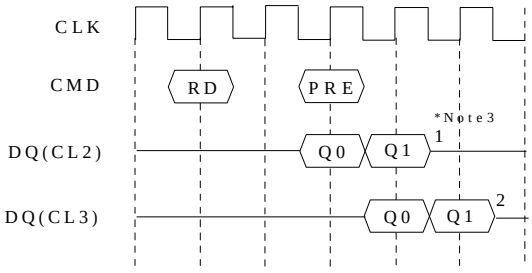
1) Write interrupted by Precharge (BL=4)



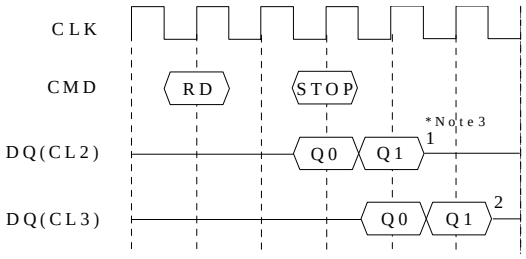
2) Write Burst Stop (Full Page Only)



3) Read interrupted by Precharge (BL=4)

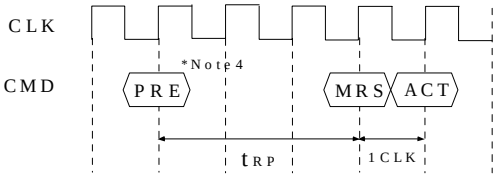


4) Read Burst Stop (Full Page Only)

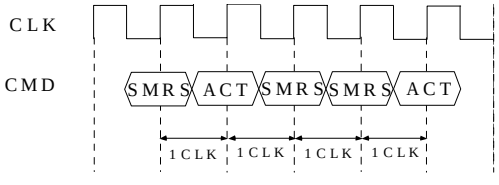


9. MRS & SMRS

1) Mode Register Set

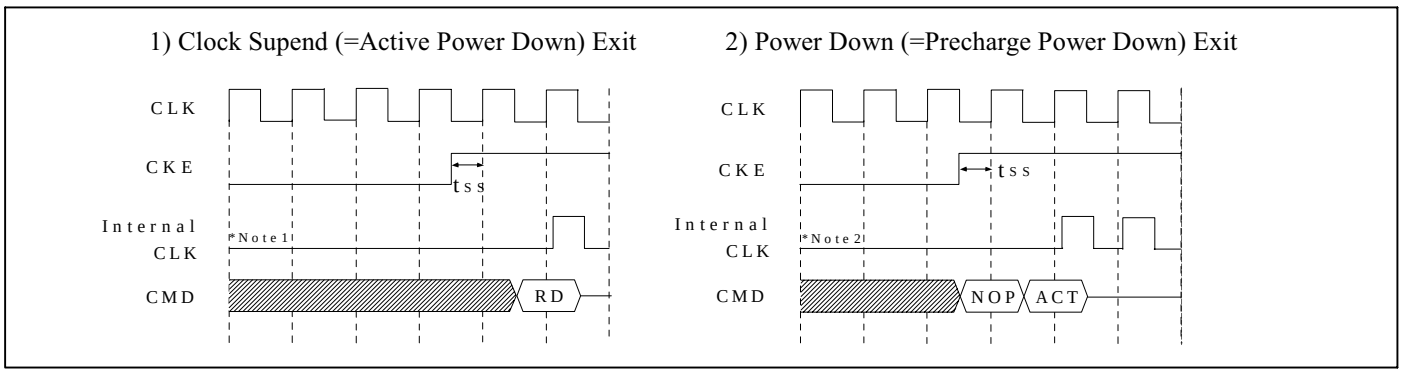


2) Special Mode Register Set

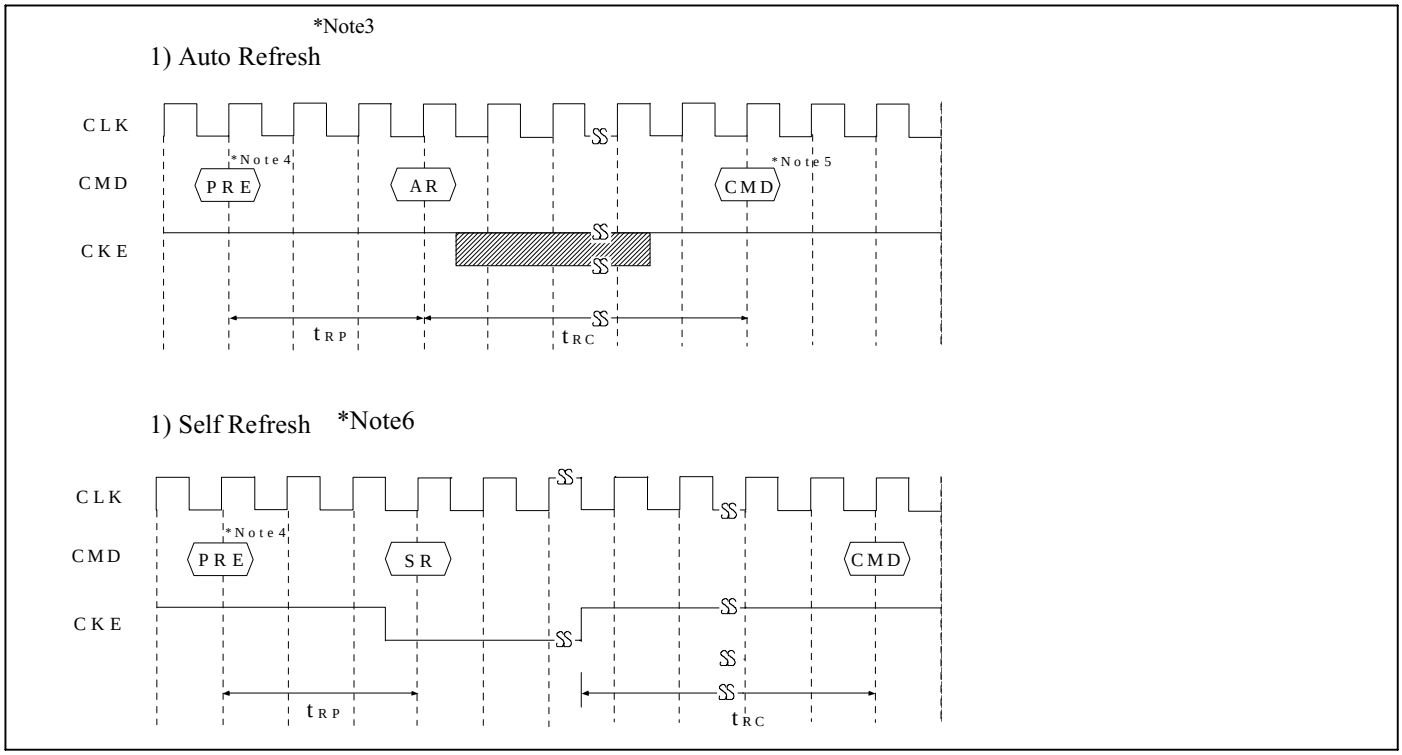


*Note: 1. t_{RDL} : 1 CLK ; Last data in to Row Precharge.
2. t_{BDL} : 1 CLK ; Last data in to Burst Stop Delay.
3. Number of valid output data after Row Precharge or burst stop : 1, 2 for CAS latency = 2, 3 respectively.
4. PRE : Both banks precharge, if necessary.
MRS can be issued only at all banks precharge state.

10. Clock Suspend Exit & Power Down Exit



11. Auto Refresh & Self Refresh



*Note : 1. Active power down : one or more banks active state.
2. Precharge power down : both banks precharge state.
3. The auto refresh is the same as CBR refresh of conventional DRAM.
No precharge commands are required after Auto Refresh command.
During t_{RC} from auto refresh command, any other command can not be accepted.
4. Before executing auto/self refresh command, both banks must be idle state.
5. (S)MRS, Bank Active, Auto/Self Refresh, Power Down Mode Entry.
6. During self refresh mode, refresh interval and refresh operation are performed internally.
After self refresh entry, self refresh mode is kept while CKE is low.

During self refresh mode, all inputs expect CKE will be don't cared, and outputs will be in Hi-Z state.
During t_{RC} from self refresh exit command, any other command can not be accepted.
Before/After self refresh mode, burst auto refresh (2K cycles) is recommended.

12. About Burst Type Control

Basic Mode	Sequential Counting	At MRS A3="0". See the BURST SEQUENCE TABLE. (BL=4, 8) BL=1, 2, 4, 8 and full page wrap around.
	Interleave Counting	At MRS A3="1". See the BURST SEQUENCE TABLE. (BL=4, 8) BL=4, 8. At BL=1, 2 Interleave Counting = Sequential Counting
Pseudo-MODE	Pseudo-Document Sequential Counting	At MRS A3="1". (See to interleave Counting Mode) Staring Address LSB 3 bits A 0-2 should be "000" or "111". @BL=8 - if LSB ="000" : Increment Counting. - if LSB ="111" : Decrement Counting. For Example, (Assume Addresses except LSB 3 bits are all 0, BL=8) -- @ write, LSB ="000", Accessed Column in order 0-1-2-3-4-5-6-7 -- @ read, LSB ="111", Accessed Column in order 7-6-5-4-3-2-1-0 At BL=4, same applications are possible. As above example, at interleave Counting mode, by confining starting address to some value, Pseudo-Decrement Counting Mode can be realize. See the BURST SEQUENCE TABLE carefully.
	Pseudo-Binary Counting	At MRS A3="0". (See to Sequential Counting Mode) A0-2 ="111". (See to Full Page Mode) Using Full Page Mode and Burst Stop Command, Binary Counting Mode can be realize. -- @ Sequential Counting, Accessed Column in order 3-4-5-6-7-1-2-3 (BL=8) -- @ Pseudo-Binary Counting Accessed Column in order 3-4-5-6-7-8-9-10 (Burst Stop command) Note. The next column address of 256 is 0.
Random MODE	Random column Access t_{CCD} = 1 CLK	Every cycle Read/Write Command with random column address can realize Random Column Access That is similar to Extended Data Out (EDO) Operation of conventional DRAM.

13. About Burst Length Control

Basic MODE	1	At MRS A2, 1, 0 ="000". At auto precharge, t_{RAS} should not be violated.
	2	At MRS A2, 1, 0 ="001". At auto precharge, t_{RAS} should not be violated.
	4	At MRS A2, 1, 0 ="010".
	8	At MRS A2, 1, 0 ="011".
	Full Page	At MRS A2, 1, 0 ="111". Wrap around mode (Infinite burst length) should be stopped by burst stop. $\overline{RAS}$ interrupt or $\overline{CAS}$ interrupt.

Special MODE	BRSW	At MRS A9 ="1" Read Burst =1, 2, 4, 8, full page/write Burst =1 At auto precharge of write, t_{RAS} should not be violated.
	Block Write	8 Column Block Write. LSB A0-2 are ignored. Burst length =1 t_{RAS} should not be violated. At auto precharge, t_{RAS} should not be violated.
Random MODE	Burst Stop	t_{BDL} =1, Valid DQ after burst stop is 1, 2 for CL=2, 3 respectively. Using burst stop command, random mode it is possible only at full page burst length.
Interrupt MODE	$\overline{RAS}$ interrupt (Interrupted by Precharge)	Before the end of burst, Row precharge command of the same bank stops read/write burst with Row precharge. t_{RDL} =1 with DQM, valid DQ after burst stop is 1, 2 for CL = 2, 3 respectively During read/write burst with auto precharge, $\overline{RAS}$ interrupt can not be issued.
	CAS Interrupt	Before the end of burst, new read/write stops read/write burst and starts new read/write burst or block write. During read/write burst with auto precharge, $\overline{CAS}$ interrupt can not be issued.

14. Mask Function

1) Normal Write

I/O masking : By Mask at Write Per Bit Mode, the selected bit planes keep the original data.

If bit plane 0, 3, 7, 9, 19, 22, 24 and 31 keep the original value.

i) STEP

I SMRS(LMR) : Load mask [31-0]="0111, 1110, 1011, 0111, 1111, 1101, 0111, 0110"

II Row Active with DSF "H" : Write Per Bit Mode Enable

III Perform Normal Write

i) ILLUSTRATION

I/O (=DQ)	31 24	23 16	15 8	7 0
External Data-in	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
DQMi	DQM3=0	DQM2=0	DQM1=0	DQM0=1
Mask Register	0 1 1 1 1 1 1 0	1 0 1 1 0 1 1 1	1 1 1 1 1 1 0 1	0 1 1 1 0 1 1 0
Before Write	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1
After Write	0 1 1 1 1 1 1 0	1 0 1 1 0 1 1 1	0 0 0 0 0 0 1 0	1 1 1 1 1 1 1 1

Note 1

2) Block Write

Pixel masking : By Pixel Data issued through DQ pin, the selected pixels keep the original data.

See PIXEL TO DQ MAPPING TABLE.

If Pixel 0, 4, 9, 13, 18, 22, 27 and 31 keep the original white color.

Assume 8bpp

White = "0000, 0000", Red = "1010, 0011", Green = "1110, 0001", Yellow = "0000, 1111", Blue = "1100, 0011"

i) STEP

I SMRS(LCR) : Load color (for 8bpp, through x32 DQ color0-3 are loaded into color registers)
Load (color3, color2, color1, color0) = (Blue, Green, Yellow, Red)
= "1100, 0011, 1110, 0001, 0000, 1111, 1010, 0011 "

II Row Active with DSF "L" : I/O Mask by Write Per Bit Mode Disable

III Block write with DQ[31-0] = "0111, 0111, 1011, 1011, 1101, 1101, 1110, 1110"

* Note : 1. DQM byte masking.

(Continued)

i) ILLUSTRATION

I/O (=DQ)		31 24	23 16	15 8	7 0
DQMi		DQM3=0	DQM2=0	DQM1=0	DQM0=1
Color Register		Color3=Blue	Color2=Green	Color1=Yellow	Color0=Red
Before Block Write & DQ (Pixel data)	000	White DQ24=H	White DQ16=H	White DQ8=H	White DQ0=L
	001	White DQ25=H	White DQ17=H	White DQ9=L	White DQ1=H
	010	White DQ26=H	White DQ18=L	White DQ10=H	White DQ2=H
	011	White DQ27=L	White DQ19=H	White DQ11=H	White DQ3=H
	100	White DQ28=H	White DQ20=H	White DQ12=H	White DQ4=L
	101	White DQ29=H	White DQ21=H	White DQ13=L	White DQ5=H
	110	White DQ30=H	White DQ22=L	White DQ14=H	White DQ6=H
	111	White DQ31=L	White DQ23=H	White DQ15=H	White DQ7=H
After Block Write	000	Blue	Green	Yellow	White
	001	Blue	Green	White	White
	010	Blue	White	Yellow	White
	011	White	Green	Yellow	White
	100	Blue	Green	Yellow	White
	101	Blue	Green	White	White
	110	Blue	White	Yellow	White
	111	White	Green	Yellow	White

Note 1

Pixel and I/O masking : By Mask at Write Per Bit Mode, the selected bit planes keep the original data.
By Pixel Data issued through DQ pin, the selected pixels keep the original data.
See PIXEL TO DQ MAPPING TABLE.

Assume 8bpp,
White = “0000, 0000”, Red = “1010, 0011”, Green = “1110, 0001”, Yellow = “0000, 1111”, Blue = “1100, 0011”

i) STEP
I SMRS(LCR) : Load color (for 8bpp, through x 32 DQ color0-3 are loaded into color registers)
Load (color3, color2, color1, color0,) = (Blue, Green, Yellow, Red)
=”1100, 0011, 1110, 0001, 0000, 1111, 1010, 0011”
II SMRS(LMR) Load mask. Mask[31-0] = ”1111.1111. 1101, 1101, 0100, 0010, 0111, 0110”
→ Byte 3 : No I/O Masking ; Byte 2 : I/O Masking ; Byte 1 : I/O and Pixel Masking ; Byte 0 : DQM Byte Masking
III Row Active with DSF “H” : I/O mask by Write Per Bit Mode Enable
IV Block Write with DQ [31-0] = ”0111, 0111 .1111, 1111, 0101, 0101, 1110, 1110 ”(Pixel Mask)

*Note : 1. At normal write, ONE column is selected among columns decorded by A2-0 (000-111).
At block write, instead of ignored address A2-0, DQ0-31 control each pixel.

i) ILLUSTRATION

I/O (=DQ)	31 24	23 16	15 6	7 0
Color Register	Blue 1 1 0 0 0 0 1 1	Green 1 1 1 0 0 0 0 1	Yellow 0 0 0 0 1 1 1 1	Red 1 0 1 0 0 0 1 1
DQMi	DQM3=0	DQM2=0	DQM1=0	DQM0=1
Mask Register	1 1 1 1 1 1 1 1	1 1 0 1 1 1 0 1	0 1 0 0 0 0 1 0	0 1 1 1 0 1 1 0
Before Write	Yellow 0 0 0 0 1 1 1 1	Yellow 0 0 0 0 1 1 1 1	Green 1 1 1 0 0 0 0 1	White 0 0 0 0 0 0 0 0
After Write	Blue 1 1 0 0 0 0 1 1	Blue 1 1 0 0 0 0 1 1	Red 1 0 1 0 0 0 1 1	White 0 0 0 0 0 0 0 0

I/O (=DQ)		31 24	23 16	15 6	7 0
DQMi		DQM3=0	DQM2=0	DQM1=0	DQM0=1
Color Register		Color3=Blue	Color2=Green	Color1=Yellow	Color0=Red
Before Block Write & DQ (Pixel data)	000	Yellow DQ24=H	Yellow DQ16=H	Green DQ8=H	White DQ0=L
	001	Yellow DQ25=H	Yellow DQ17=H	Green DQ9=L	White DQ1=H
	010	Yellow DQ26=H	Yellow DQ18=H	Green DQ10=H	White DQ2=H
	011	Yellow DQ27=L	Yellow DQ19=H	Green DQ11=L	White DQ3=H
	100	Yellow DQ28=H	Yellow DQ20=H	Green DQ12=H	White DQ4=L
	101	Yellow DQ29=H	Yellow DQ21=H	Green DQ13=L	White DQ5=H
	110	Yellow DQ30=H	Yellow DQ22=H	Green DQ14=H	White DQ6=H
	111	Yellow DQ31=L	Yellow DQ23=H	Green DQ15=L	White DQ7=H
After Block Write	000	Blue	Blue	Red	White
	001	Blue	Blue	Green	White
	010	Blue	Blue	Red	White
	011	Yellow	Blue	Green	White
	100	Blue	Blue	Red	White
	101	Blue	Blue	Green	White
	110	Blue	Blue	Red	White
	111	Yellow	Blue	Green	White
	Note 2				Note 1
		PIXEL MASK	I/O MASK	PIXEL & I/O MASK	BYTE MASK

*Note : 1. DQM byte masking.

2. At normal write, ONE column is selected among columns decorded by A2-0(000-111)
At block write, instead of ignored address A2-0, DQ0-31 control each pixel.

FUNCTION TRUTH TABLE (TABLE 1)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	BA	ADDR	ACTION	Note
IDLE	H	X	X	X	X	X	X	NOP	
	L	H	H	H	X	X	X	NOP	
	L	H	H	L	X	X	X	ILLEGAL	2
	L	H	L	X	X	BA	CA	ILLEGAL	2
	L	L	H	H	L	BA	RA	Row Active ; Latch Row Address ; Non-IO Mask	
	L	L	H	H	H	BA	RA	Row Active ; Latch Row Address ; IO Mask	
	L	L	H	L	L	X	PA	Auto Refresh or Self Refresh	4
	L	L	H	L	H	BA	X	NOP	
	L	L	L	H	L	X	X	Auto Refresh or Self Refresh	5
	L	L	L	H	H	BA	X	ILLEGAL	
	L	L	L	L	L	OP Code		Mode Register Access	5
	L	L	L	L	H	OP Code		Special Mode Register Access	6
Row Active	H	X	X	X	X	X	X	NOP	
	L	H	H	H	X	X	X	NOP	
	L	H	H	L	X	X	X	ILLEGAL	2
	L	H	L	H	L	BA	CA, AP	Begin Read ; Latch CA ; Determine AP	
	L	H	L	H	H	X	X	ILLEGAL	
	L	H	L	L	L	BA	CA, AP	Begin Write ; Latch CA ; Determine AP	
	L	H	L	L	H	BA	CA, AP	Begin Write ; Latch CA ; Determine AP	
	L	L	H	H	X	BA	RA	ILLEGAL	2
	L	L	H	L	L	BA	RA	Precharge	
	L	L	H	L	H	X	X	ILLEGAL	
	L	L	L	H	X	X	X	ILLEGAL	
	L	L	L	L	L	X	X	ILLEGAL	
	L	L	L	L	H	OP Code		Special Mode Register Access	6
Read	H	X	X	X	X	X	X	NOP (Continue Burst to End → Row Active)	
	L	H	H	H	X	X	X	NOP (Continue Burst to End → Row Active)	
	L	H	H	L	L	X	X	Term burst → Row active	
	L	H	H	L	H	X	X	ILLEGAL	
	L	H	L	H	L	BA	CA, AP	Term burst, Begin Read ; Latch CA ; Determine AP	3
	L	H	L	H	H	X	X	ILLEGAL	
	L	H	L	L	L	BA	CA, AP	Term burst, Begin Write ; Latch CA ; Determine AP	3
	L	H	L	L	H	BA	CA, AP	Term burst, Begin Write ; Latch CA ; Determine AP	3
	L	L	H	H	X	BA	RA	ILLEGAL	2
	L	L	H	L	L	BA	PA	Term Burst, Precharge timing for Reads	3
	L	L	H	L	H	X	X	ILLEGAL	
	L	L	L	X	X	X	X	ILLEGAL	
Write	H	X	X	X	X	X	X	NOP (Continue Burst to End → Row Active)	
	L	H	H	H	X	X	X	NOP (Continue Burst to End → Row Active)	
	L	H	H	L	L	X	X	Term burst → Row Active	
	L	H	H	L	H	X	X	ILLEGAL	
	L	H	L	H	L	BA	CA, AP	Term burst, Begin Read ; Latch CA ; Determine AP	3
	L	H	L	H	H	X	X	ILLEGAL	
	L	H	L	L	L	BA	CA, AP	Term burst, Begin Write ; Latch CA ; Determine AP	3
	L	H	L	L	H	BA	CA, AP	Term burst, Begin Write ; Latch CA ; Determine AP	3

FUNCTION TRUTH TABLE (TABLE 1, Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	BA	ADDR	ACTION	Note
Write	L	L	H	H	X	BA	RA	ILLEGAL	2
	L	L	H	L	L	BA	RA	Term Burst : Precharge timing for Writes	3
	L	L	H	H	H	X	X	ILLEGAL	
	L	L	L	X	X	X	X	ILLEGAL	
Read with Auto Precharge	H	X	X	X	X	X	X	NOP(Continue Burst to End → Precharge)	
	L	H	H	H	X	X	X	NOP(Continue Burst to End → Precharge)	
	L	H	H	L	X	X	X	ILLEGAL	
	L	H	L	H	X	BA	CA, AP	ILLEGAL	2
	L	H	L	L	X	BA	CA, AP	ILLEGAL	2
	L	L	H	X	X	BA	RA, PA	ILLEGAL	
	L	L	L	X	X	X	X	ILLEGAL	2
Write with Auto Precharge	H	X	X	X	X	X	X	NOP(Continue Burst to End → Precharge)	
	L	H	H	H	X	X	X	NOP(Continue Burst to End → Precharge)	
	L	H	H	L	X	X	X	ILLEGAL	
	L	H	L	H	X	BA	CA, AP	ILLEGAL	2
	L	H	L	L	X	BA	CA, AP	ILLEGAL	2
	L	L	H	X	X	BA	RA, PA	ILLEGAL	
	L	L	L	X	X	X	X	ILLEGAL	2
Precharging	H	X	X	X	X	X	X	NOP → Idle after t_{RP}	
	L	H	H	H	X	X	X	NOP → Idle after t_{RP}	
	L	H	H	L	X	X	X	ILLEGAL	
	L	H	L	X	X	BA	CA, AP	ILLEGAL	2
	L	L	H	H	X	BA	RA	ILLEGAL	2
	L	L	H	L	X	BA	PA	NOP → Idle after t_{RP}	2
	L	L	L	X	X	X	X	ILLEGAL	4
Block Write Recovering	H	X	X	X	X	X	X	NOP → Row Active after t_{BWC}	
	L	H	H	H	X	X	X	NOP → Row Active after t_{BWC}	
	L	H	H	L	X	X	X	ILLEGAL	
	L	H	L	X	X	BA	CA, AP	ILLEGAL	2
	L	L	H	H	X	BA	RA	ILLEGAL	2
	L	L	H	L	X	BA	PA	Term Block Write : Precharge timing for Block Write	2
	L	L	L	X	X	X	X	ILLEGAL	2
Row Activating	H	X	X	X	X	X	X	NOP → Row Active after t_{RCD}	
	L	H	H	H	X	X	X	NOP → Row Active after t_{RCD}	
	L	H	H	L	X	X	X	ILLEGAL	
	L	H	L	X	X	BA	CA, AP	ILLEGAL	2
	L	L	H	H	X	BA	RA	ILLEGAL	2
	L	L	H	L	X	BA	PA	ILLEGAL	2
	L	L	L	X	X	X	X	ILLEGAL	2
Refreshing	H	X	X	X	X	X	X	NOP → Idle after t_{RC}	
	L	H	H	X	X	X	X	NOP → Idle after t_{RC}	
	L	H	L	X	X	X	X	ILLEGAL	
	L	L	H	X	X	X	X	ILLEGAL	
	L	L	L	X	X	X	X	ILLEGAL	

ABBREVIATIONS :

RA = Row Address (A0~A10) BA = Bank Address (BA) PA = Precharge All (A8)
NOP = No Operation Command CA = Column Address (A0~A7) AP = Auto Precharge (A8)

FUNCTION TRUTH TABLE (TABLE 1, Continued)

*Note : 1. All entries assume the CKE was active (High) during the preceding clock cycle and the current clock cycle.
2. Illegal to bank in specified state ; Function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA (and PA).
5. Illegal if any bank is not idle.
6. Legal only if all banks are in idle or row active state.

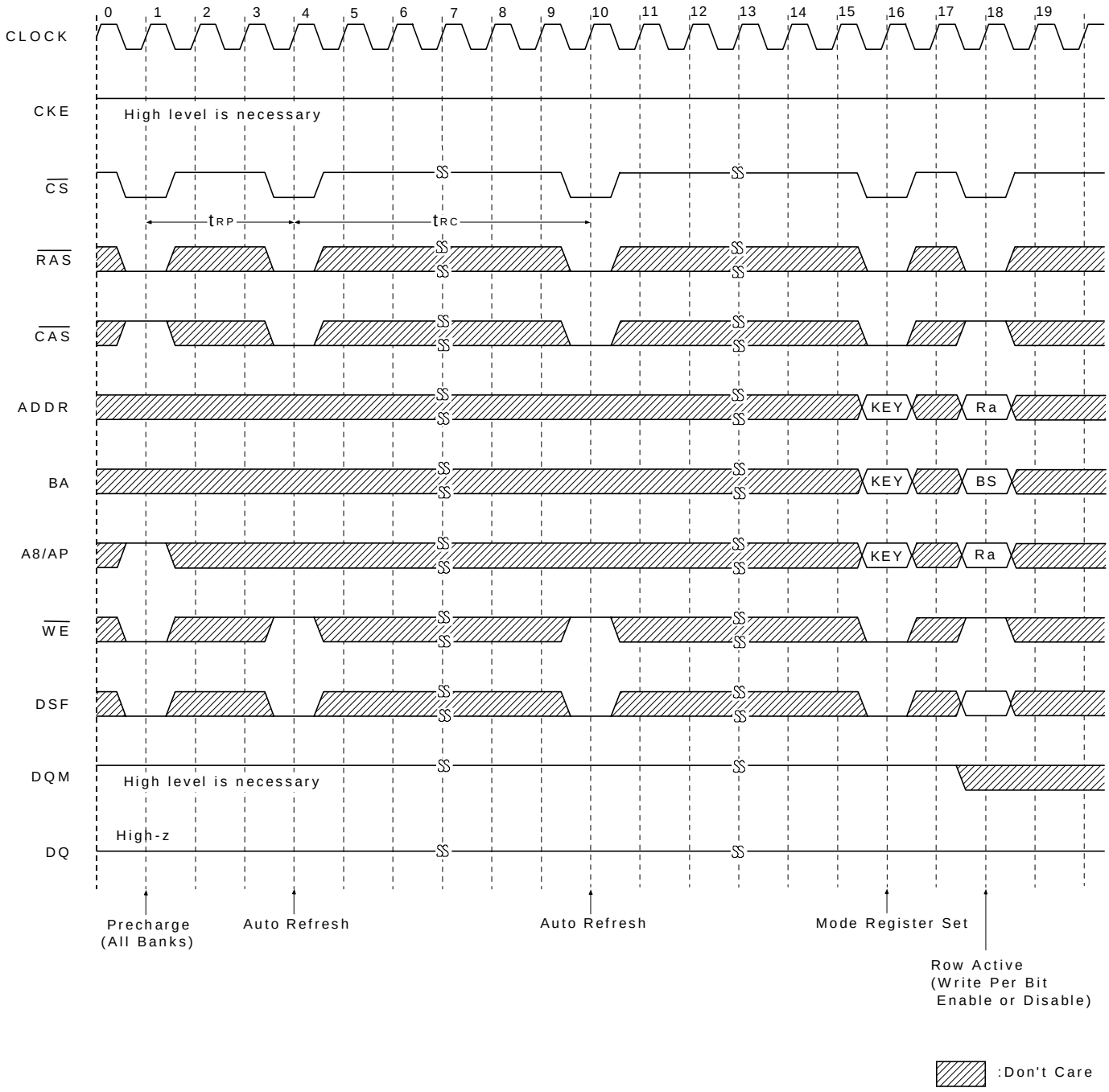
FUNCTION TRUTH TABLE for CKE (TABLE2)

Current State	CKE (n-1)	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	ADDR	ACTION	Note
Self Refresh	H	X	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	X	Exit Self Refresh →ABI after t_{RC}	7
	L	H	L	H	H	H	X	X	Exit Self Refresh →ABI after t_{RC}	7
	L	H	L	H	H	L	X	X	ILLEGAL	
	L	H	L	H	L	X	X	X	ILLEGAL	
	L	H	L	L	X	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	X	NOP (Maintain Self Refresh)	
Both Bank Precharge Power Down	H	X	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	X	Exit Power Down →ABI	8
	L	H	L	H	H	H	X	X	Exit Power Down →ABI	8
	L	H	L	H	H	L	X	X	ILLEGAL	
	L	H	L	H	L	X	X	X	ILLEGAL	
	L	H	L	L	X	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	X	NOP (Maintain Low Power Mode)	
All Banks Idle	H	H	X	X	X	X	X	X	Refer to Table 1	
	H	L	H	X	X	X	X	X	Enter Power Down	9
	H	L	L	H	H	H	X	X	Enter Power Down	9
	H	L	L	H	H	L	X	X	ILLEGAL	
	H	L	L	H	L	X	X	X	ILLEGAL	
	H	L	L	L	H	X	X	X	ILLEGAL	
	H	L	L	L	L	H	X	X	Enter Self Refresh	9
	H	L	L	L	L	L	X	X	ILLEGAL	
	L	L	X	X	X	X	X	X	NOP	
Any State other than Listed Above	H	H	X	X	X	X	X	X	Refer to Operations in Table 1	
	H	L	X	X	X	X	X	X	Begin Clock Suspend next cycle	10
	L	H	X	X	X	X	X	X	Exit Clock Suspend next cycle	10
	L	L	X	X	X	X	X	X	Maintain Clock Suspend	

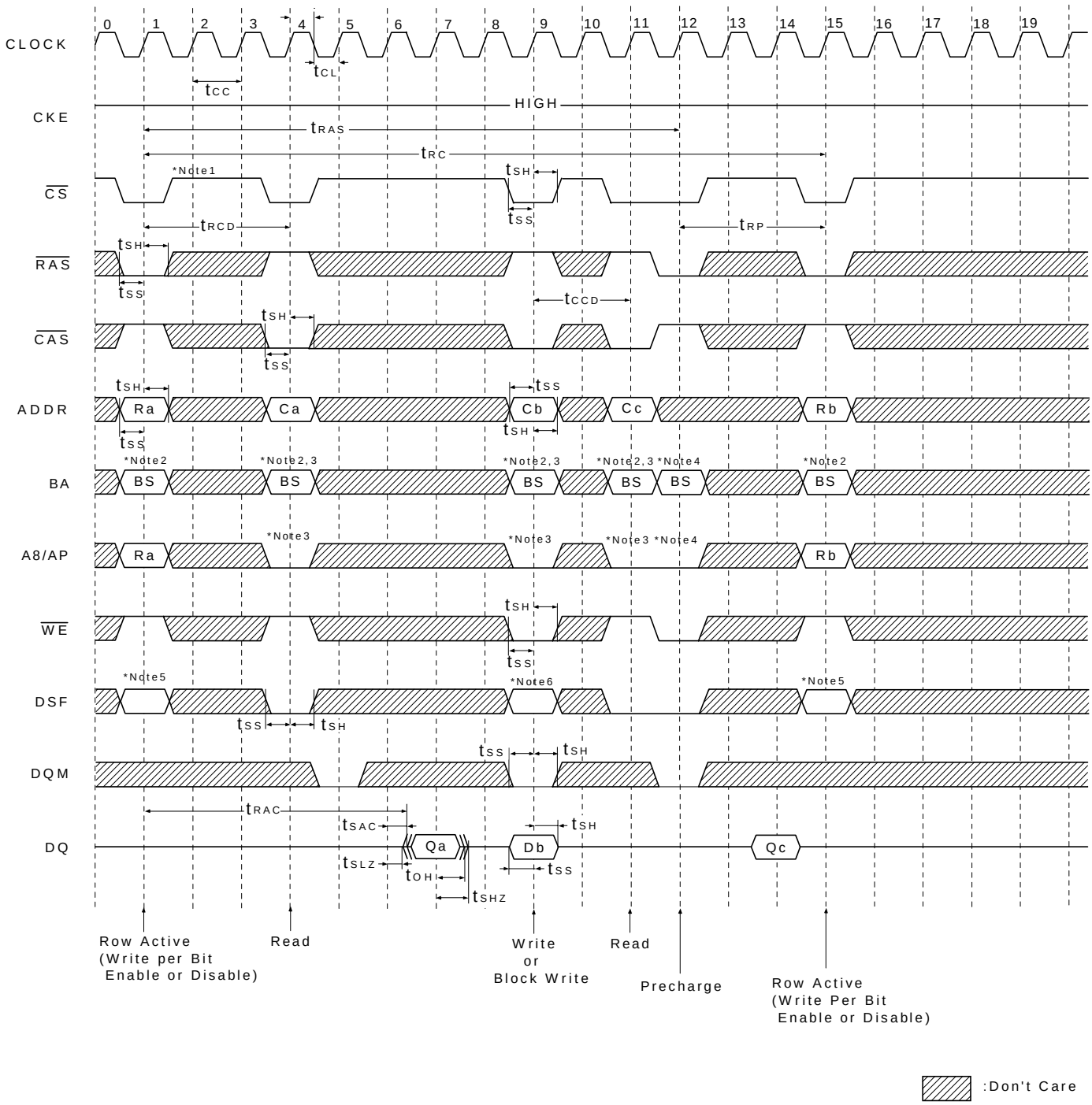
ABBREVIATIONS : ABI = All Banks Idle

*Note : 7.After CKE's low to high transition to exit self refresh mode. And a time of $t_{RC(min)}$ has to be elapse after CKE's low to high transition to issue a new command.
8.CKE low to high transition is asynchronous as if restart internal clock.
A minimum setup time " t_{SS} + one clock " must be satisfy before any command other than exit.
9.Power down and self refresh can be entered only from the all banks idle state.
10.Must be a legal command.

Power On Sequence & Auto Refresh



Single Bit Read-Write-Read Cycle (Same Page) @CAS Latency = 3, Burst Length = 1



* Note : 1. All input can be don't care when $\overline{CS}$ is high at the CLK high going edge.
2. Bank active & read/write are controlled by BA.

BA	Active & Read/Write
0	Bank A
1	Bank B

3. Enable and disable auto precharge function are controlled by A8/AP in read/write command.

A8/AP	BA	Operation
0	0	Disable auto precharge, leave bank A active at end of burst.
	1	Disable auto precharge, leave bank B active at end of burst.
1	0	Enable auto precharge, precharge bank A at end of burst.
	1	Enable auto precharge, precharge bank B at end of burst.

4. A8/AP and BA control bank precharge when precharge command is asserted.

A8/AP	BA	Precharge
0	0	Bank A
0	1	Bank B
1	X	Both Bank

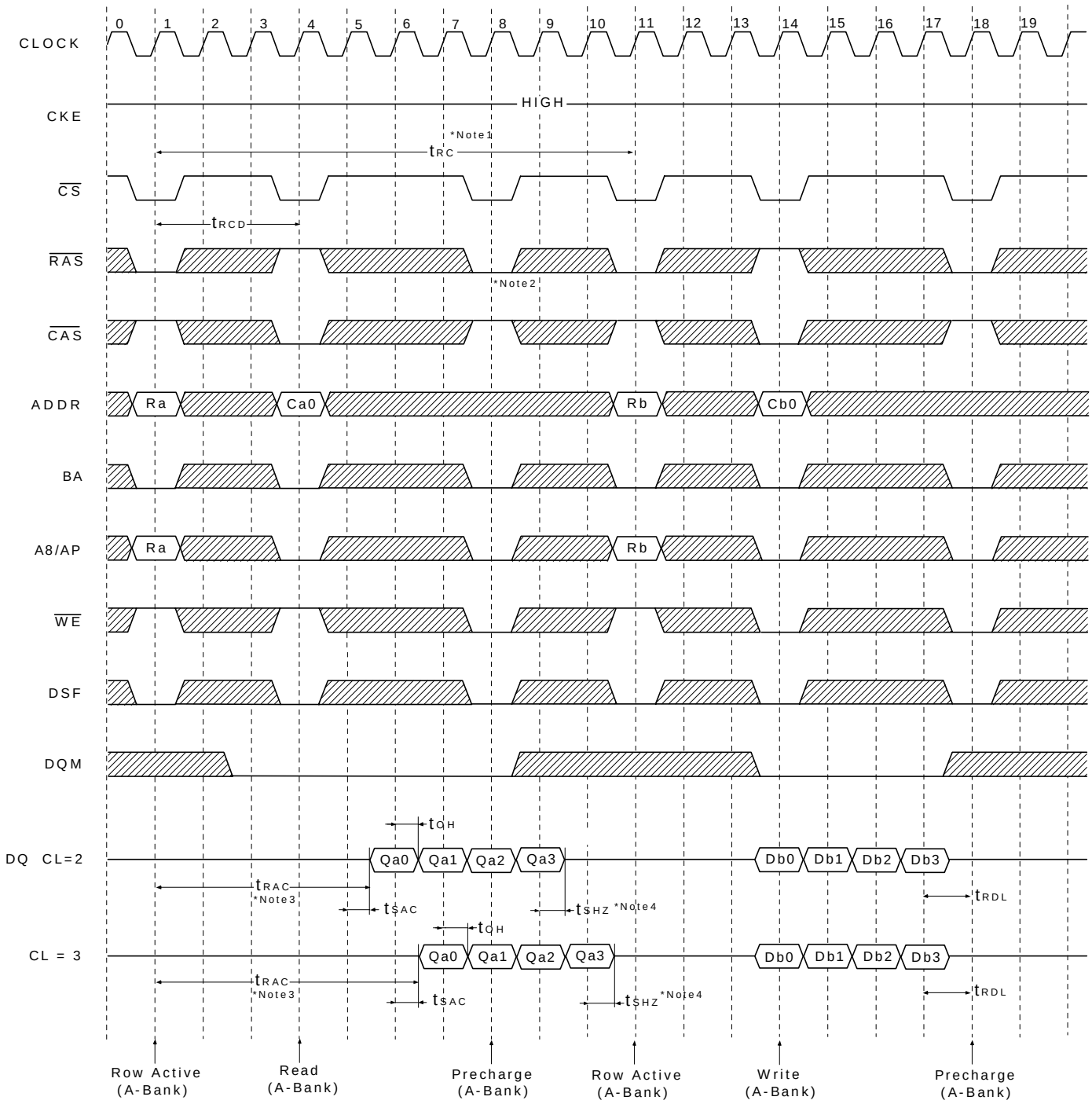
5. Enable and disable Write-per Bit function are controlled by DSF in Row Active command.

BA	DSF	Operation
0	L	Bank A row active, disable write per bit function for bank A.
	H	Bank A row active, enable write per bit function for bank A.
1	L	Bank B row active, disable write per bit function for bank B.
	H	Bank B row active, enable write per bit function for bank B.

6. Block write/normal write is controlled by DSF.

DSF	Operation	Minimum cycle time
L	Normal write	t_{CCD}
H	Block write	t_{BWC}

Read & Write Cycle at Same Bank @ Burst Length = 4



:Don't Care

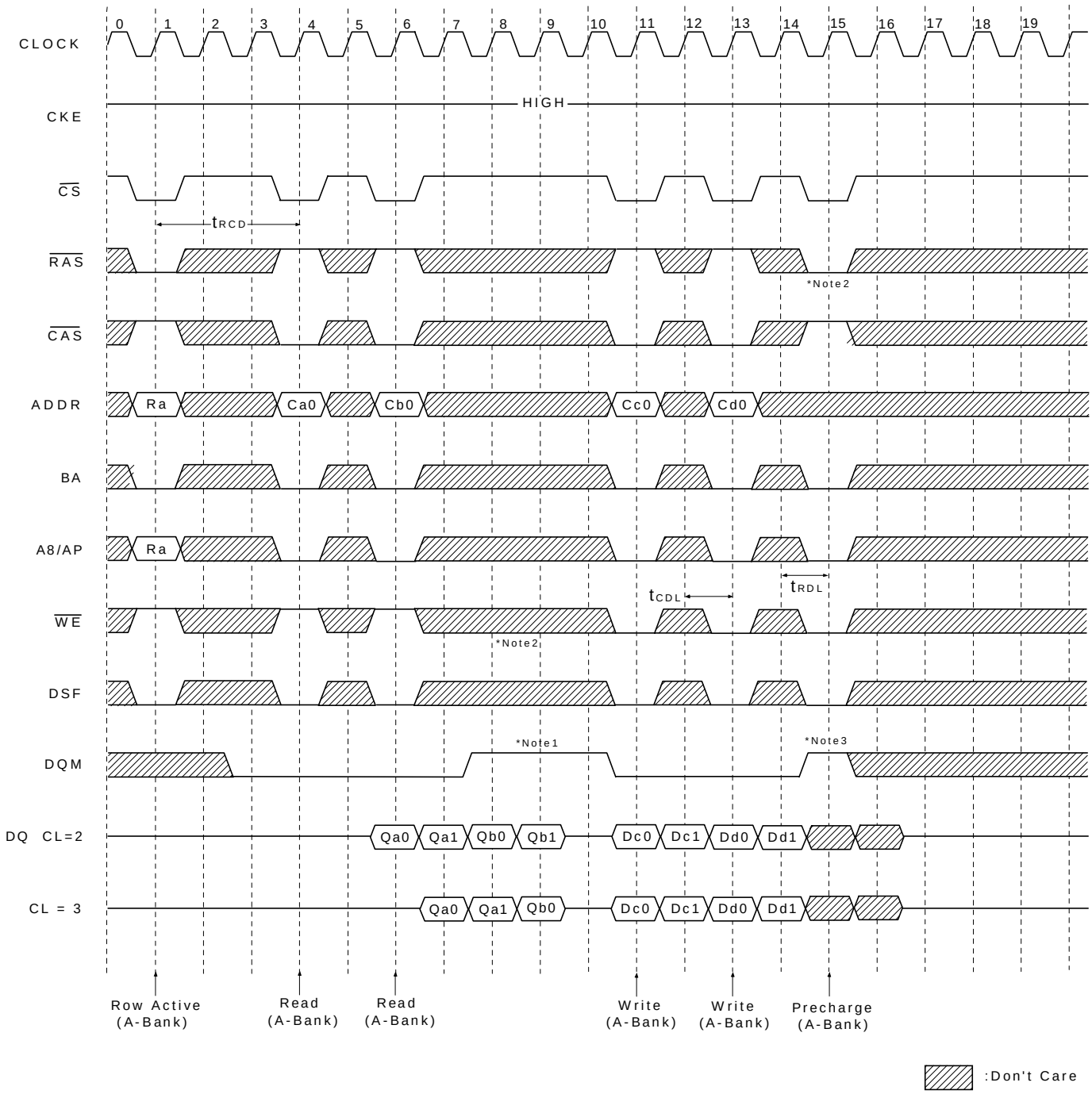
*Note : 1. Minimum row cycle time is required to complete internal DRAM operation.

2. Row precharge can interrupt burst on any cycle.[CAS Length - 1] valid output data available after Row. enters precharge. Last valid output will be Hi-Z after t_{SHZ} from the clock.

3. Access time from Row address. t_{CC} *(t_{RCD} +CAS latency - 1) + t_{SAC}

4. Output will be Hi-Z after the end of burst. (1, 2, 4 & 8)
At Full page bit burst, burst is wrap-around.

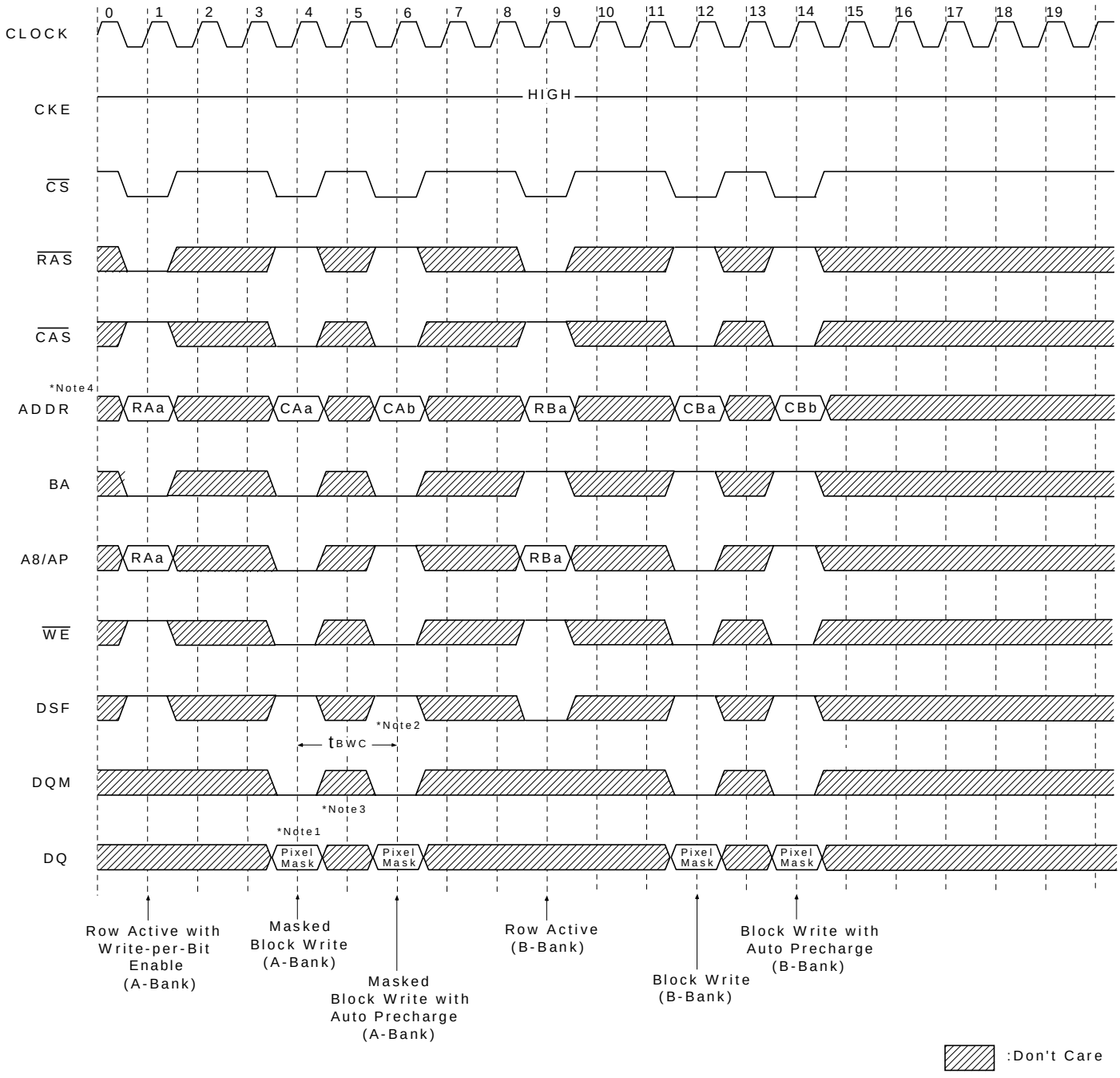
Page Read & Write Cycle Same Bank @ Burst Length = 4



* Note : 1.To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.

2. Row precharge will interrupt writing. Last data input, t_{RDL} before Row precharge, will be written.
3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

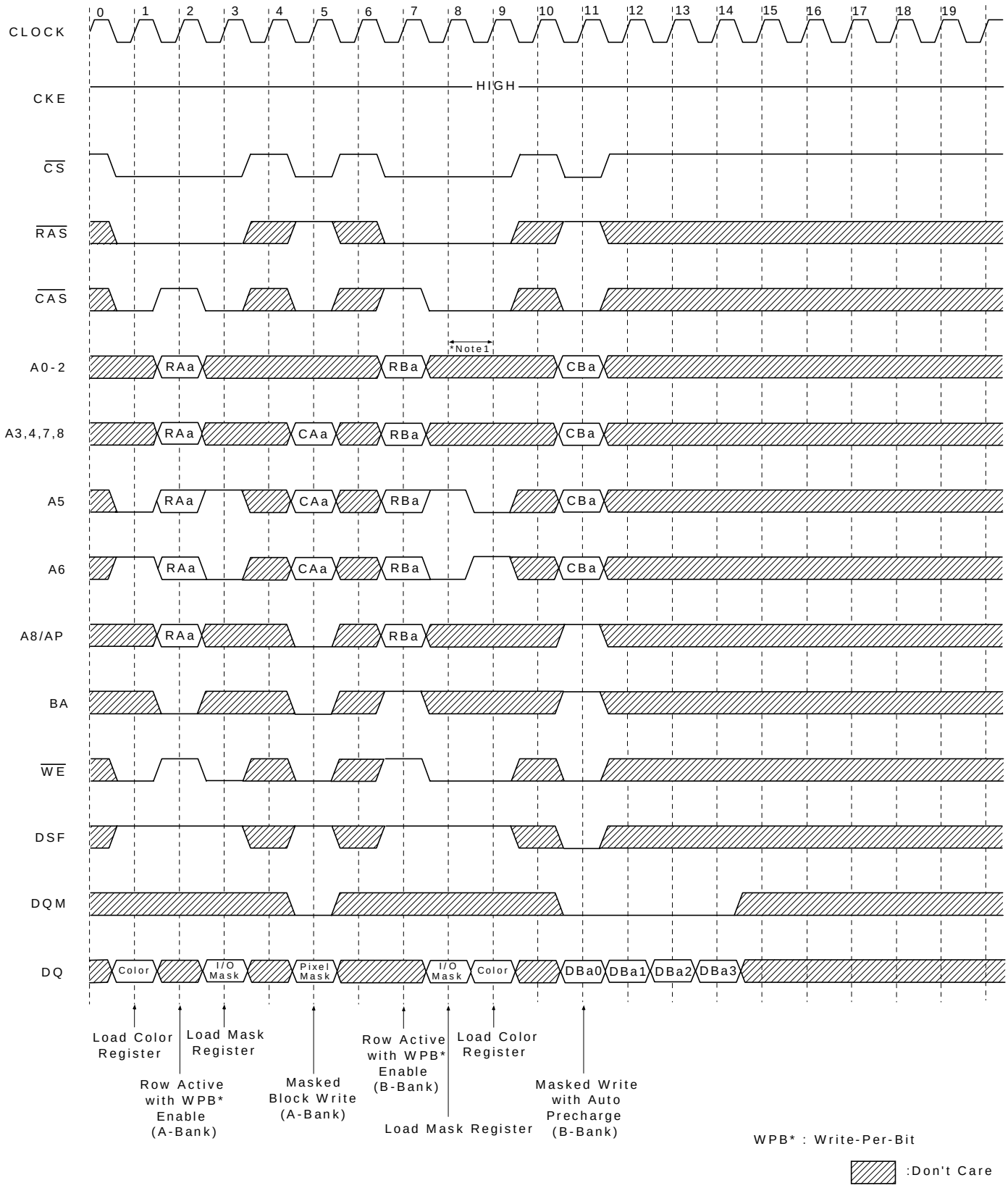
Block Write cycle (with Auto Precharge)



*Note : 1. Column Mask (DQi = L : Mask, DQi = H : Non Mask)

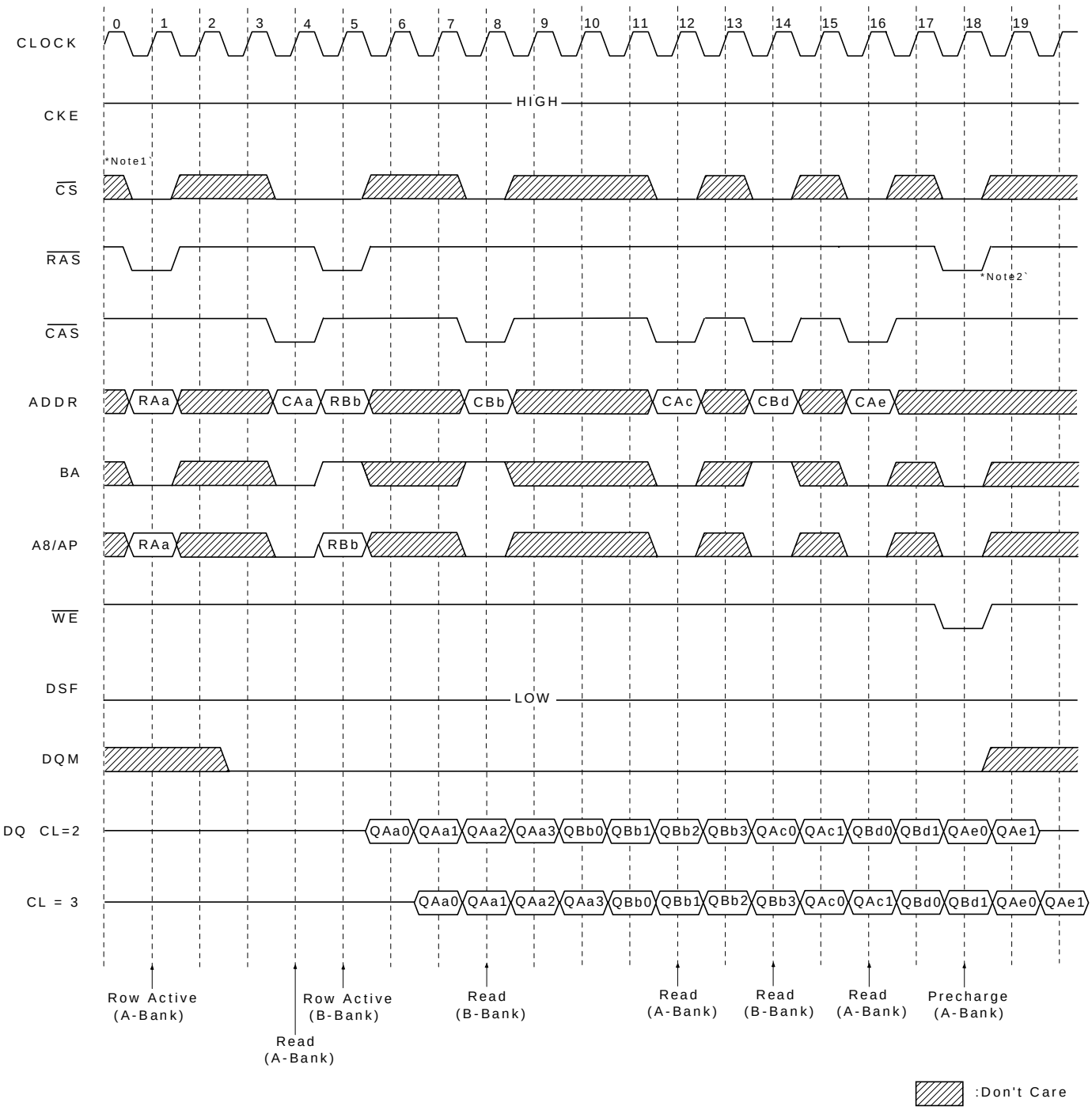
2. t_{BWC} : Block Write Cycle time
3. At Block Write, second cycle should be in NOP.
   Other Bank can be active or precharge.
4. At Block Write. CA0-2 are ignored.

SMRS and Block/Normal Write @ Burst Length = 4



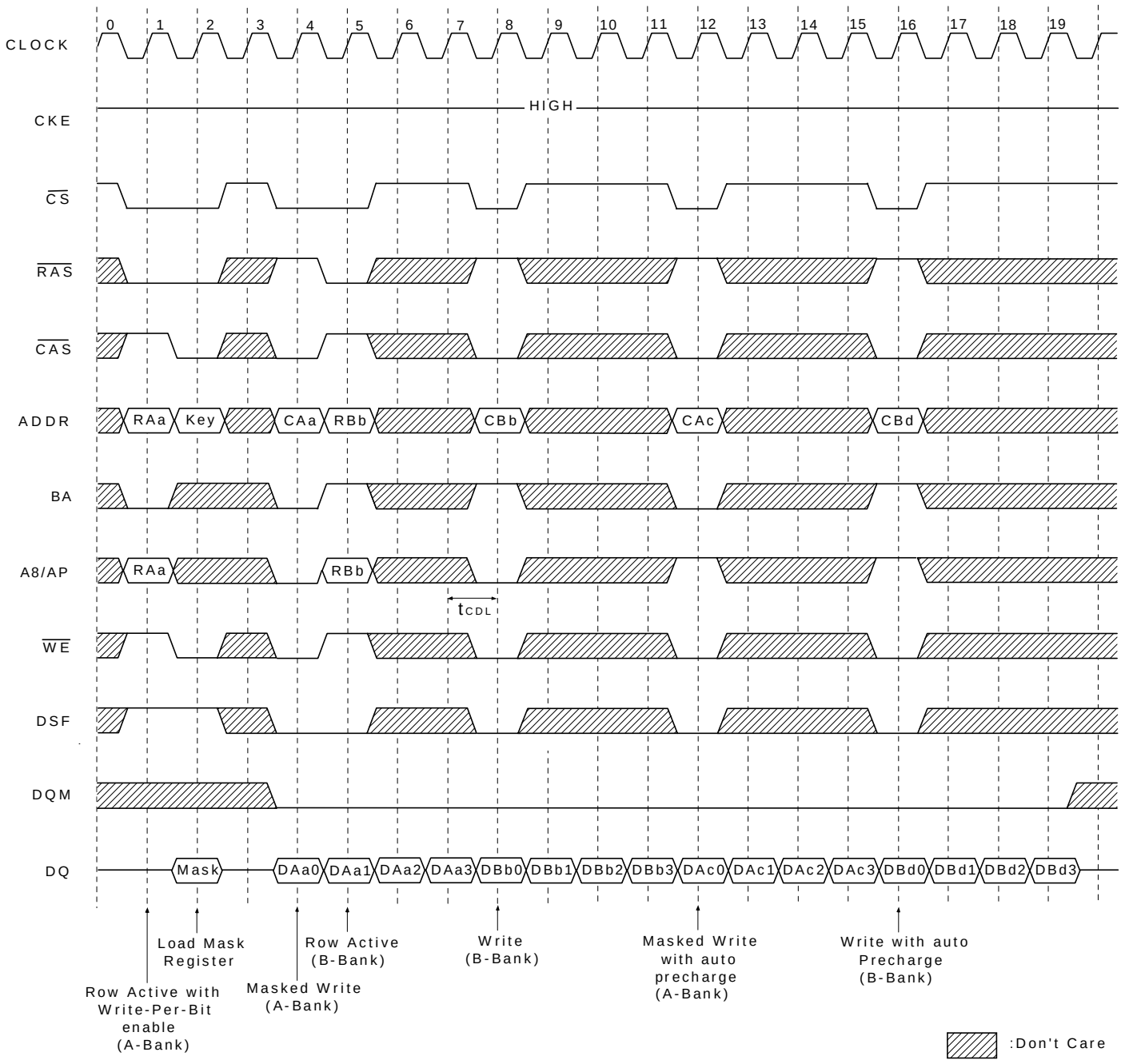
*Note : 1. At the next clock of special mode register set command, new command is possible.

Page Read Cycle at Different Bank @ Burst Length = 4

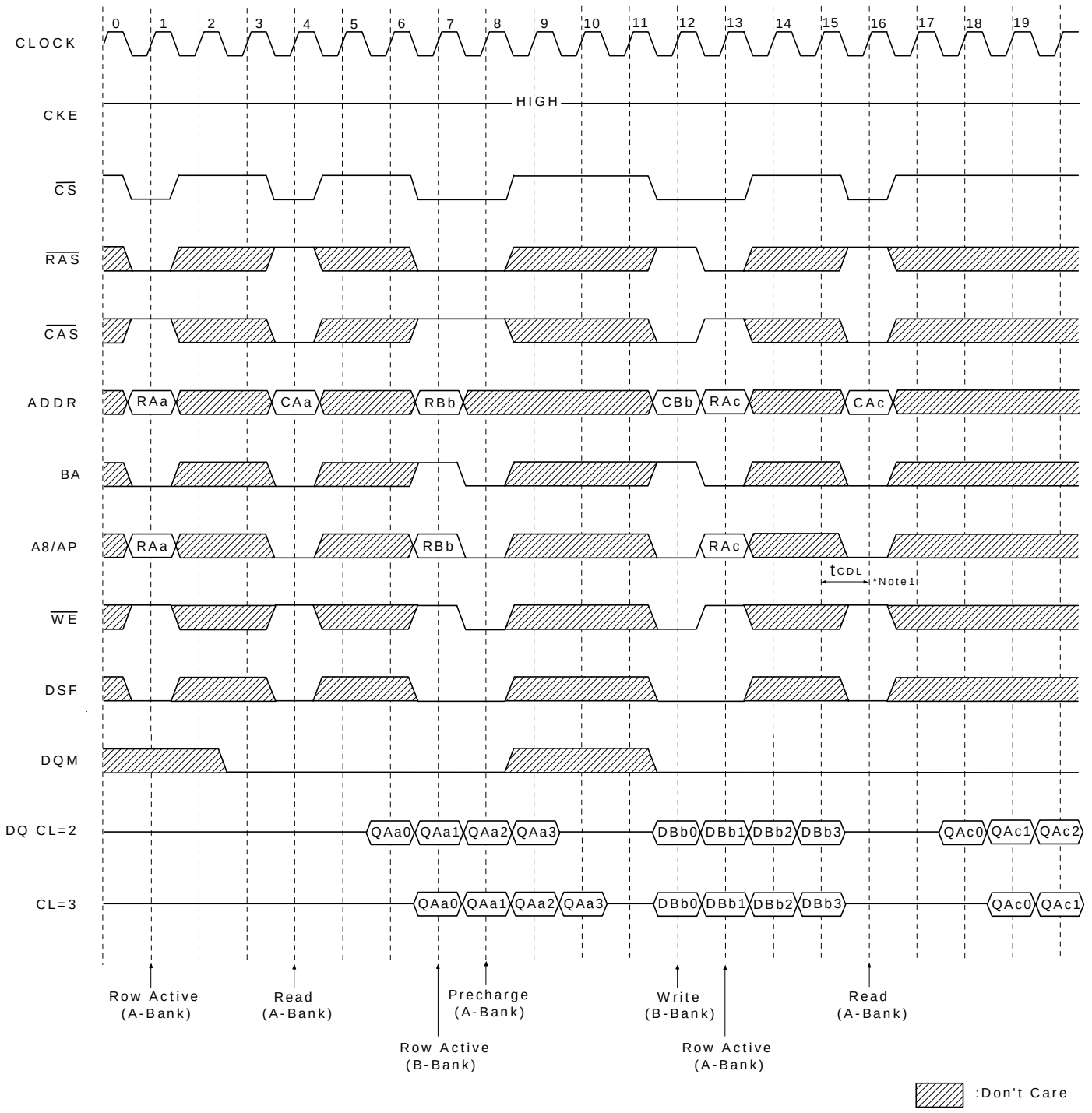


*Note : 1. $\overline{CS}$ can be don't care when $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high at the clock high going edge.
2. To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

Page Write Cycle at Different Bank @ Burst Length =4

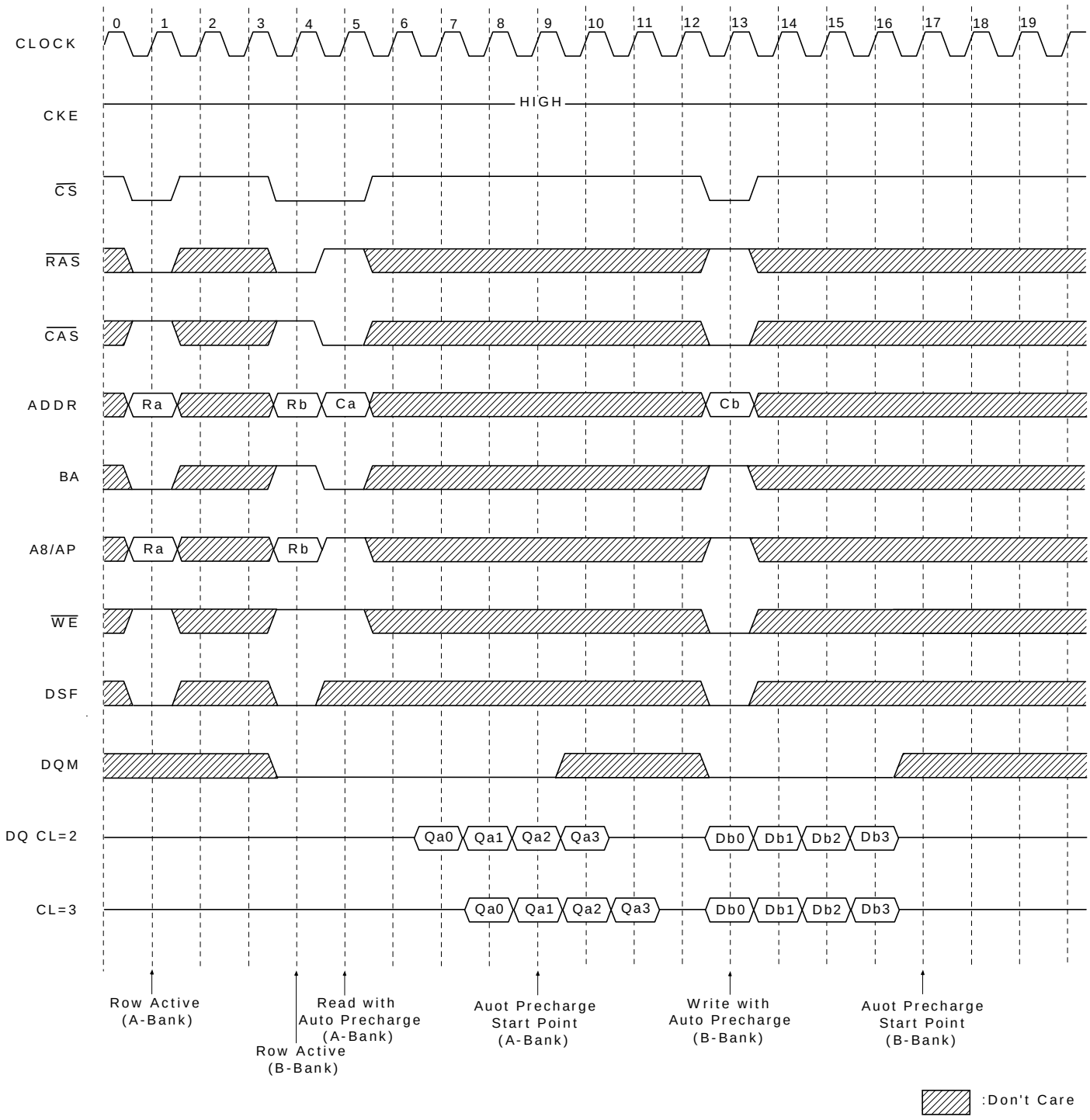


Read & Write Cycle at Different Bank @ Burst Length =4



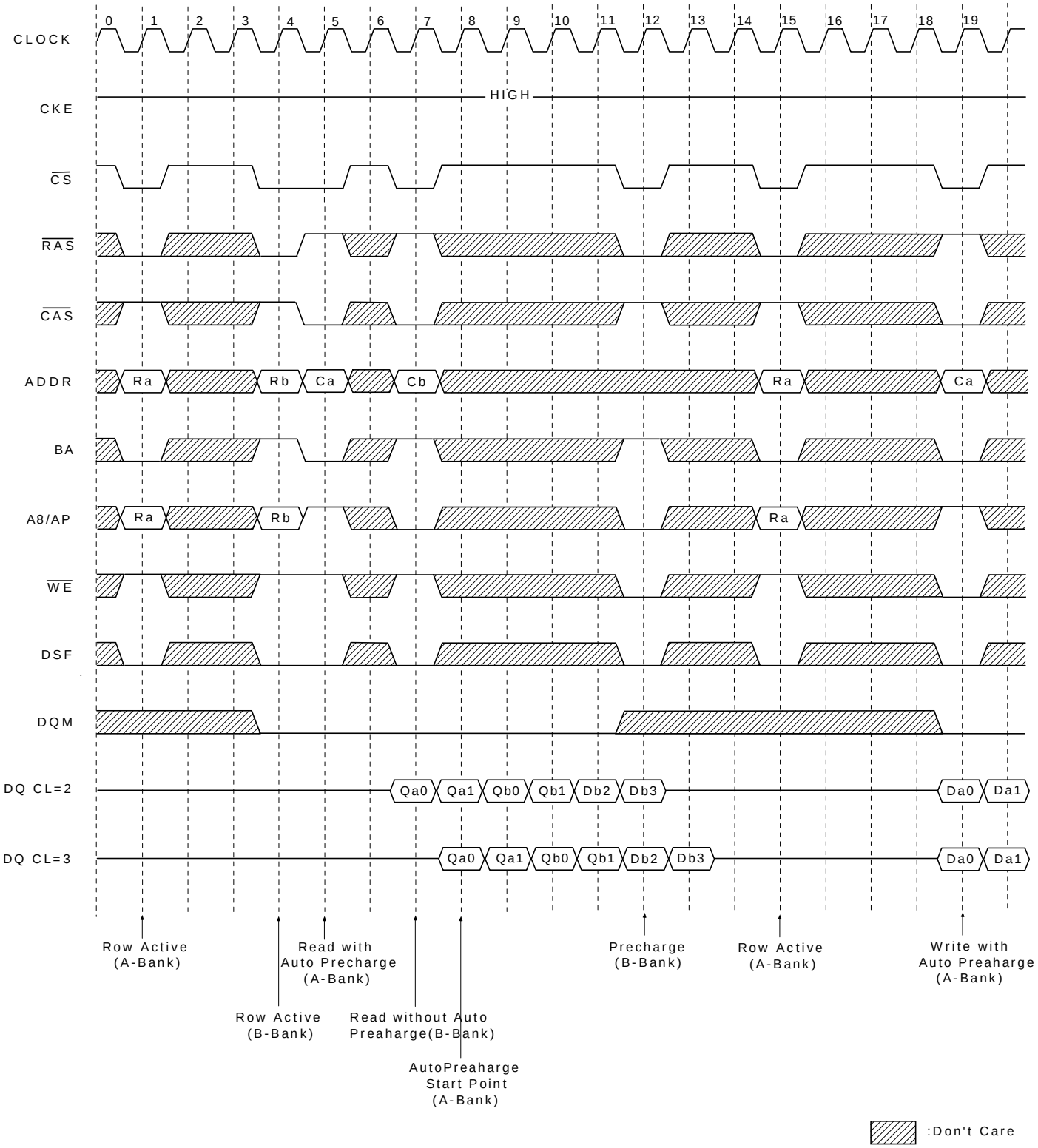
*Note : 1. t_{CDL} should be met to complete write.

Read & Write Cycle with Auto Precharge @ Burst Length =4



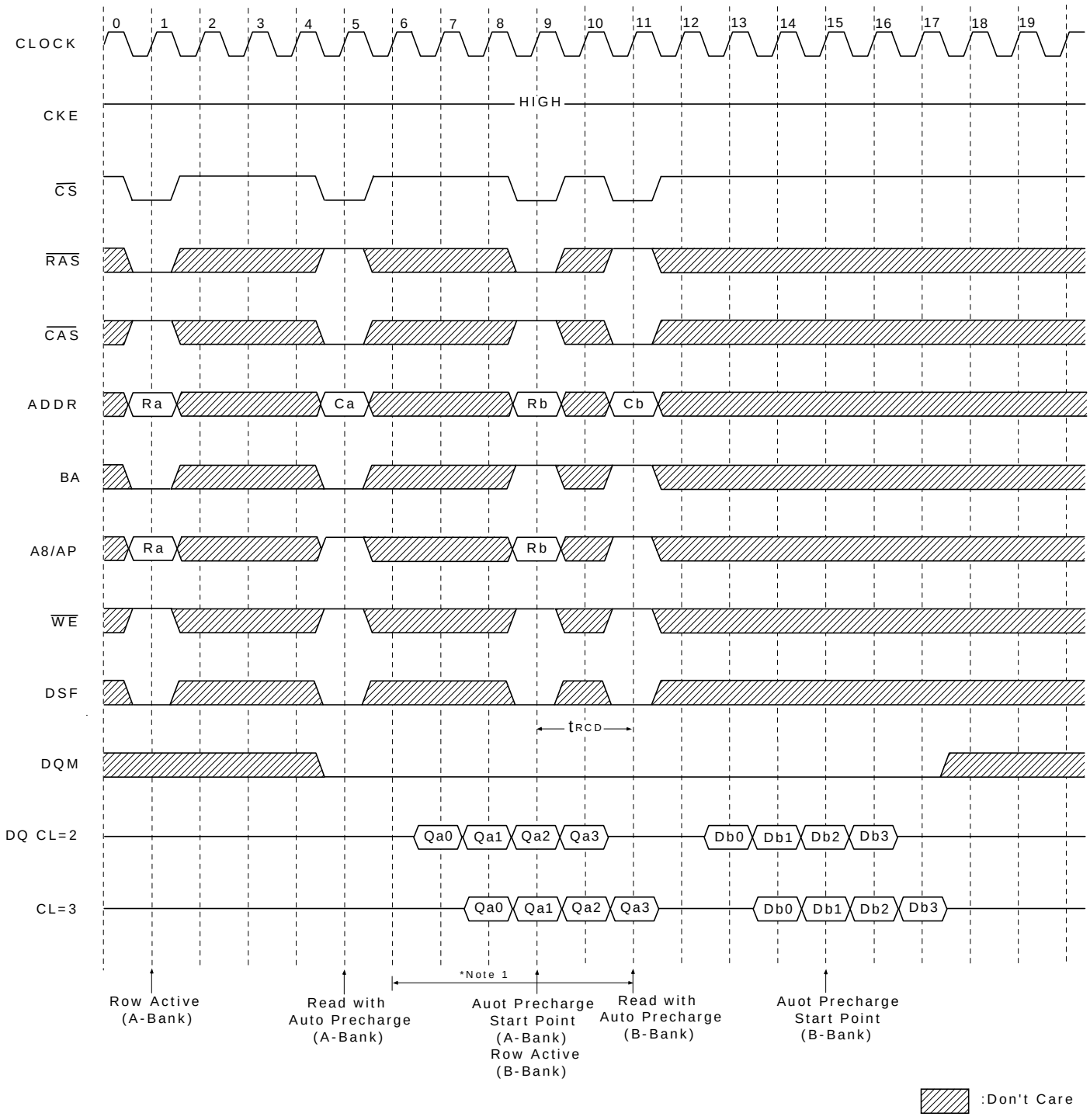
*Note : 1. t_{RDL} should be controlled to meet minimum t_{RAS} before internal precharge start.
(In the case of Burst Length = 1 & 2, BRSW mode and Block write)

Read & Write Cycle with Auto Precharge II @ Burst Length =4



*Note : 1. When Read(Write) command with auto precharge is issued at A-Bank after A and B Bank activation.
- If Read(Write) command without auto precharge is issued at B-Bank before A Bank auto precharge starts, A Bank auto precharge will start at the next cycle of B Bank read command input point.
- any command can not be issued at A Bank during t_{RP} after A Bank auto precharge starts.

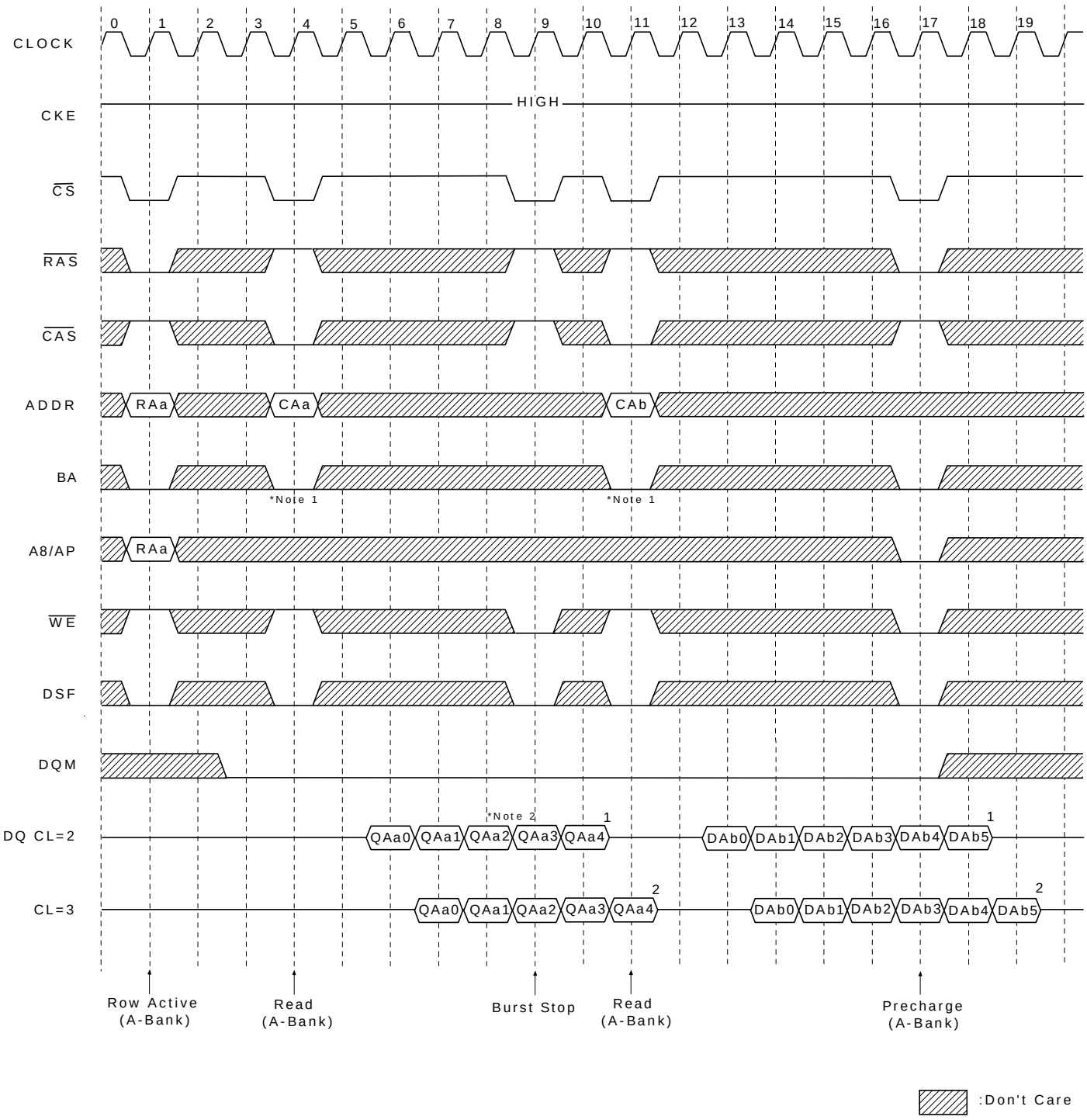
Read & Write Cycle with Auto Precharge III @ Burst Length =4



*Note : 1. Any command to A Bank is not allowed in this period.

t_{RP} is determined from at auto precharge start point.

Read Interrupted by Precharge Command & Read Burst Stop Cycle (@ Full Page Only)

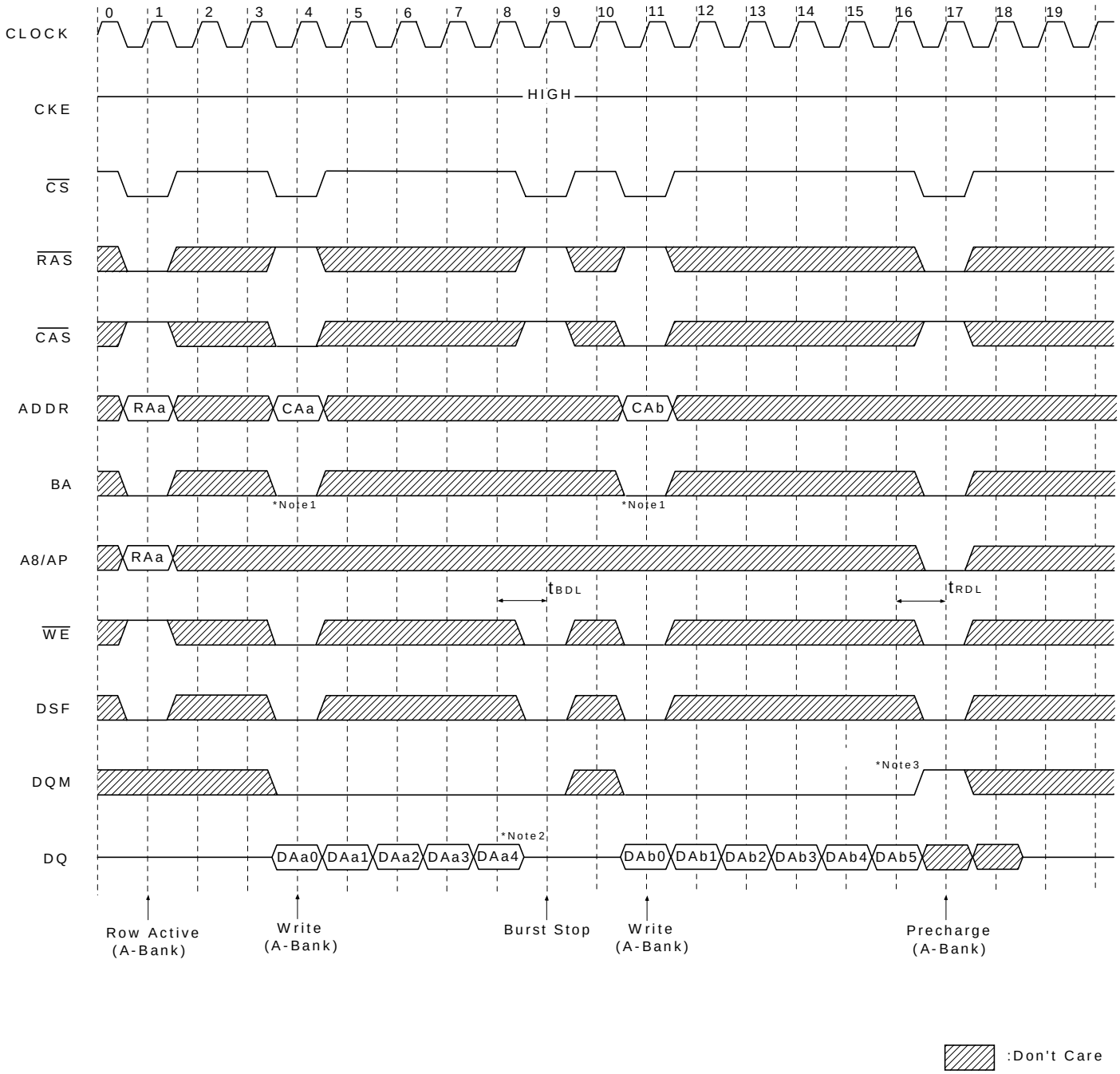


*Note : 1. At full page mode, burst is warp-around at the end of burst. So auto precharge is impossible.

2. About the valid DQ's after burst stop, it is same as the case of $\overline{RAS}$ interrupt.
Both cases are illustrated above timing diagram. See the label 1, 2 on them.
But at burst write, Burst stop and $\overline{RAS}$ interrupt should be compared carefully.
Refer the timing diagram of "Full page write burst stop cycle".

3. Burst stop is valid at full page mode.

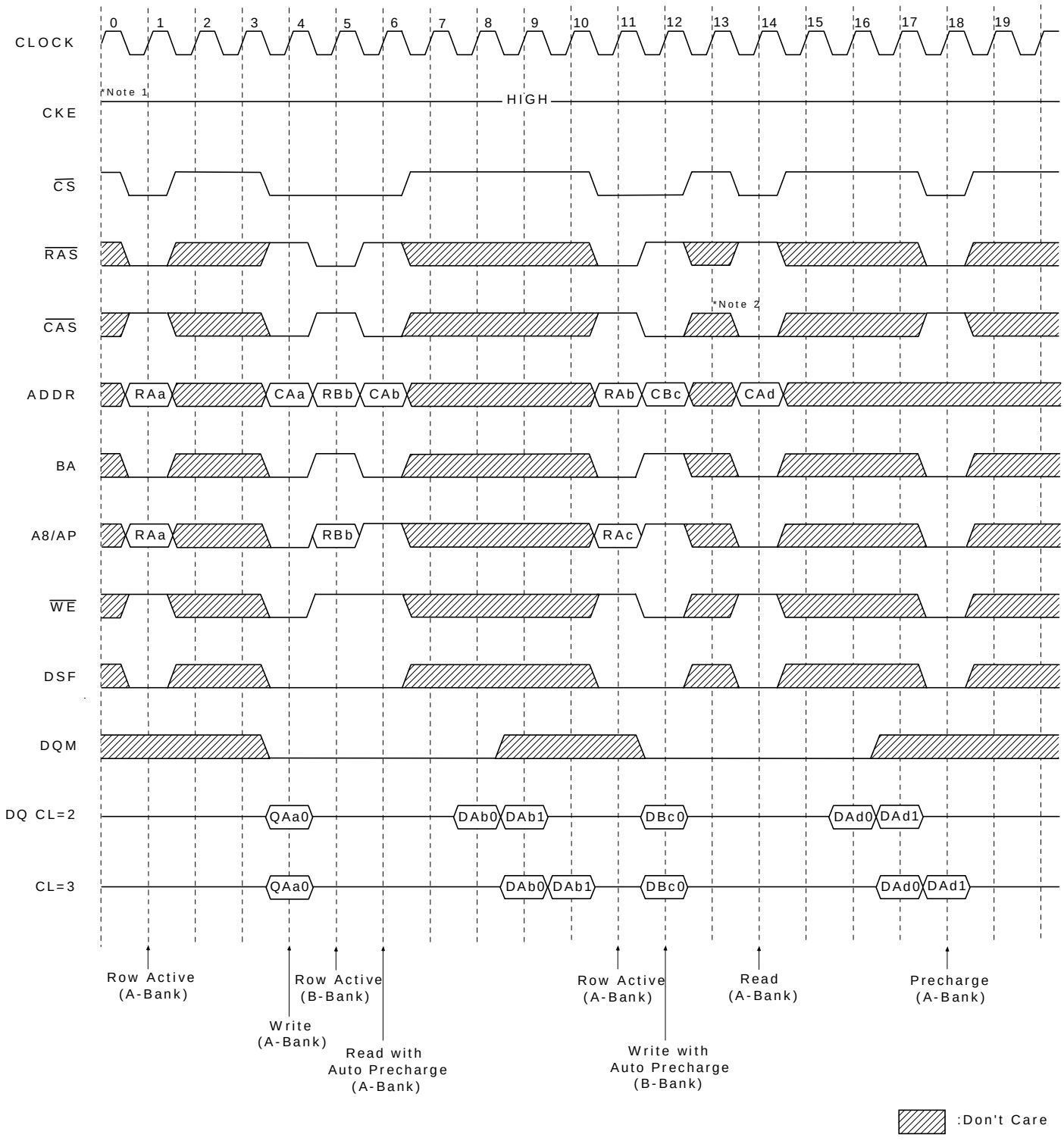
Write Interrupted by Precharge Command & Write Burst Stop Cycle (@ Full Page Only)



*Note : 1. At full page mode, burst is warp-around at the end of burst. So auto precharge is impossible.

2. Data-in at the cycle of burst stop command cannot be written into the corresponding memory cell.
   It is defined by AC parameter of t_{BDL} (=1CLK).
3. Data-in at the cycle interrupted by precharge cannot be written into the corresponding memory cell.
   It is defined by AC parameter of t_{RDL} (=1CLK).
   DQM at write interrupted by precharge command is needed to ensure t_{RDL} of 1CLK.
   DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst.
   Input data after Row precharge cycle will be masked internally.
4. Burst stop is valid only at full page burst length.

Burst Read Single bit Write Cycle @ Burst Length = 2, BRSW

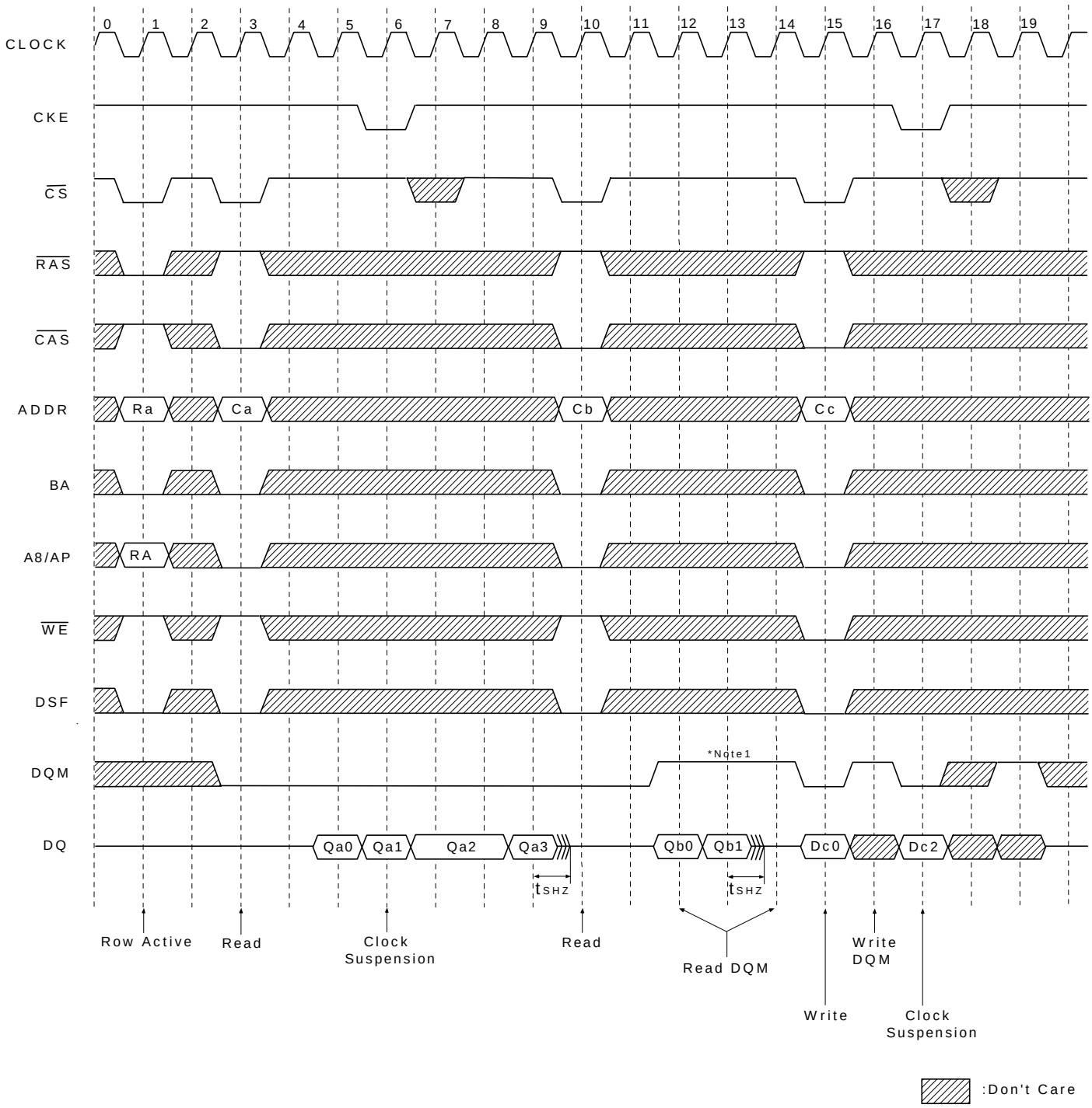


*Note : 1. BRSW mode is enabled by setting A9 "High" at MRS (Mode Register Set).
At the BRSW Mode, the burst length at write is fixed to "1" regardless of programed burst length.

2. When BRSW write command with auto precharge is executed, keep it in mind that t_{RAS} should not be violated.
Auto precharge is executed at the burst-end cycle, so in the case of BRSW write command.
The next cycle is also starts the precharge.

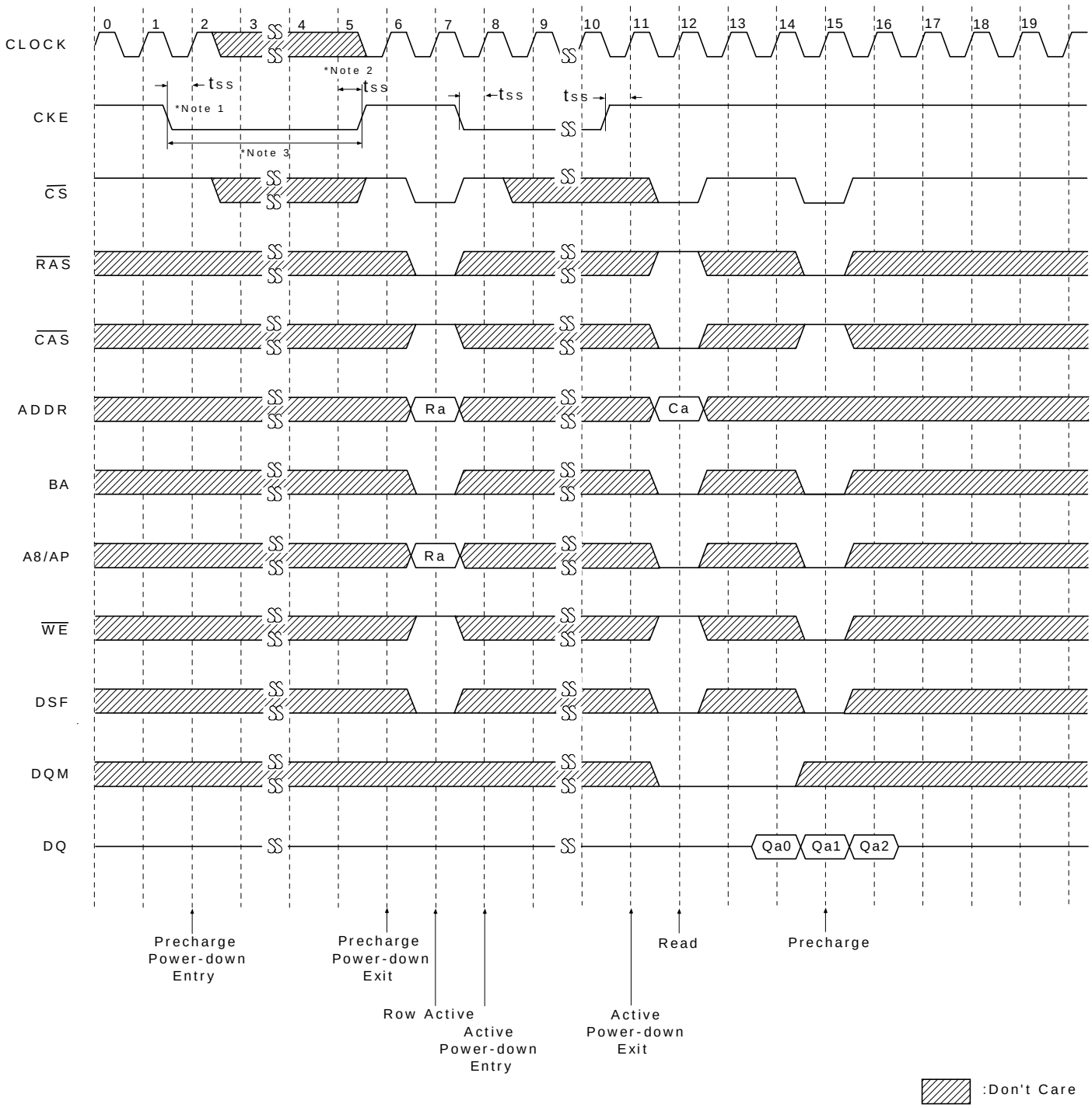
3. WPB function is also possible at BRSW mode.

Clock suspension & DQM operation cycle @ CAS Latency = 2, Burst Length = 4



*Note : 1. DQM needed to prevent bus contention.

Active/Precharge Power Down Mode @ CAS Latency = 2, Burst Length =4

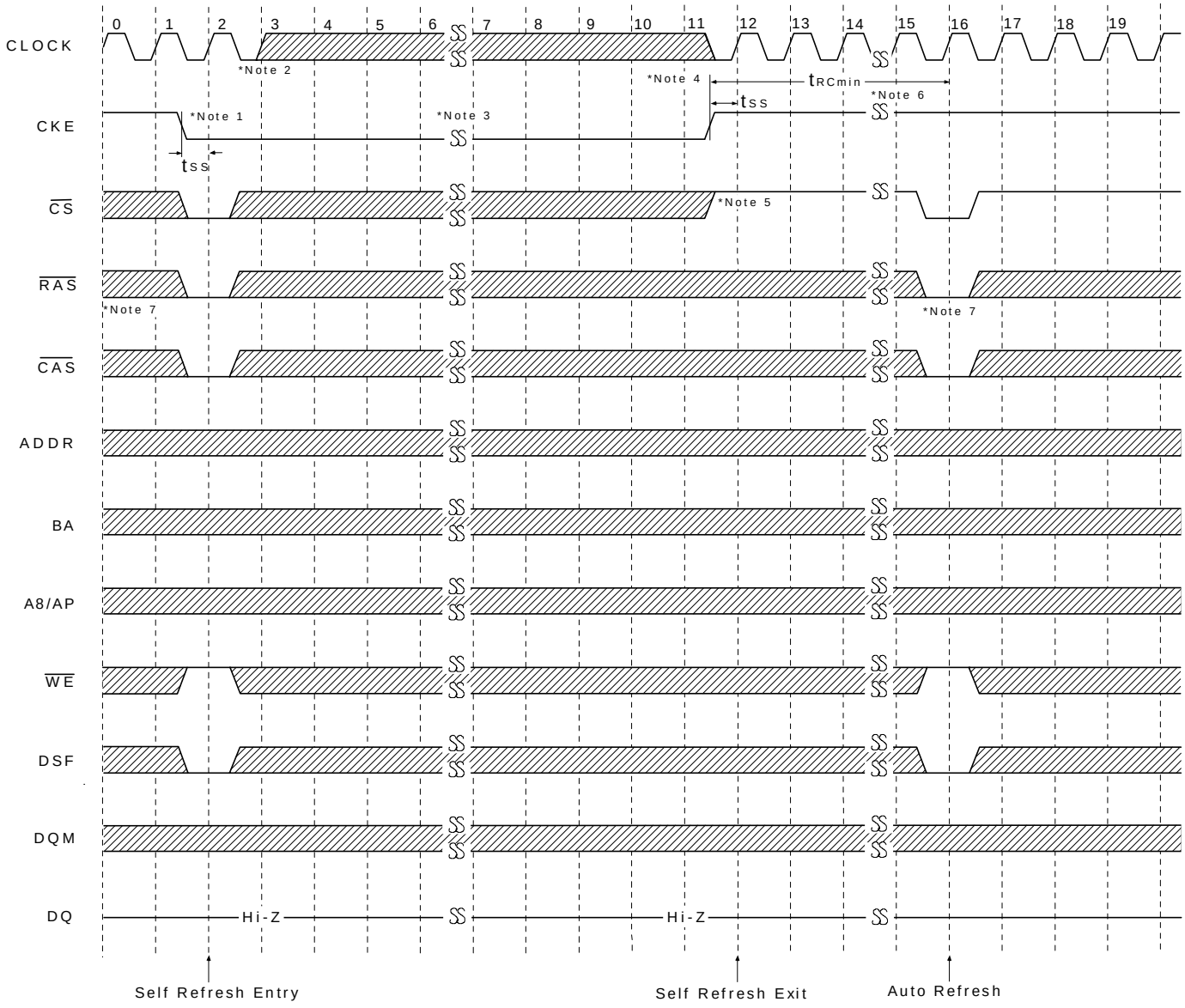


*Note : 1. All banks should be in idle state prior to entering precharge power down mode.

2. CKE should be set high at lease "1CLK + tss" prior to Row active command.

3. Cannot violate minimum refresh specification. (32ms)

Self Refresh Entry & Exit Cycle



*Note : TO ENTER SELF REFRESH MODE

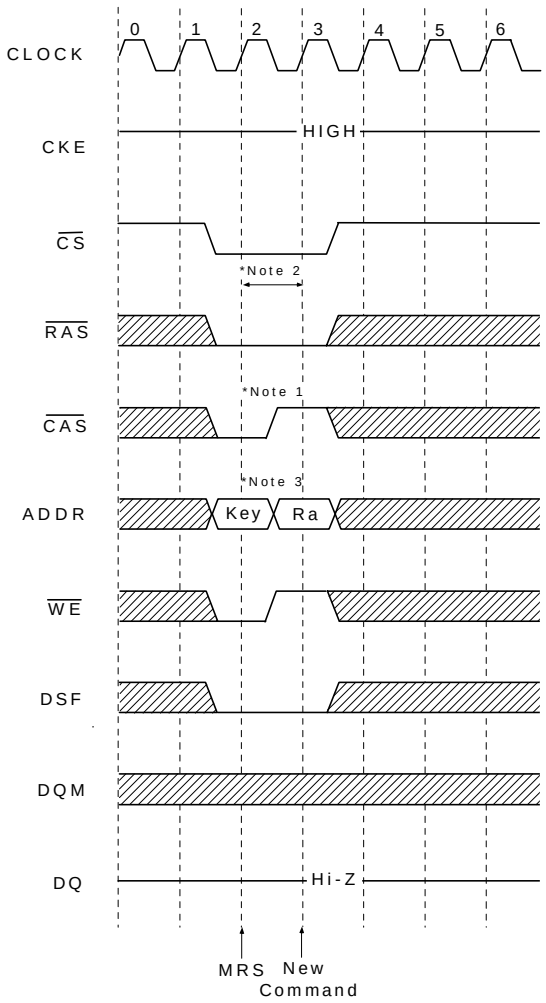
1. $\overline{CS}$, $\overline{RAS}$ & $\overline{CAS}$ with CKE should be low at the same clock cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don't care except for CKE.
3. The device remains in self refresh mode as long as CKE stays "Low".

   cf.) Once the device enters self refresh mode minimum t_{RAS} is required before exit from self refresh.

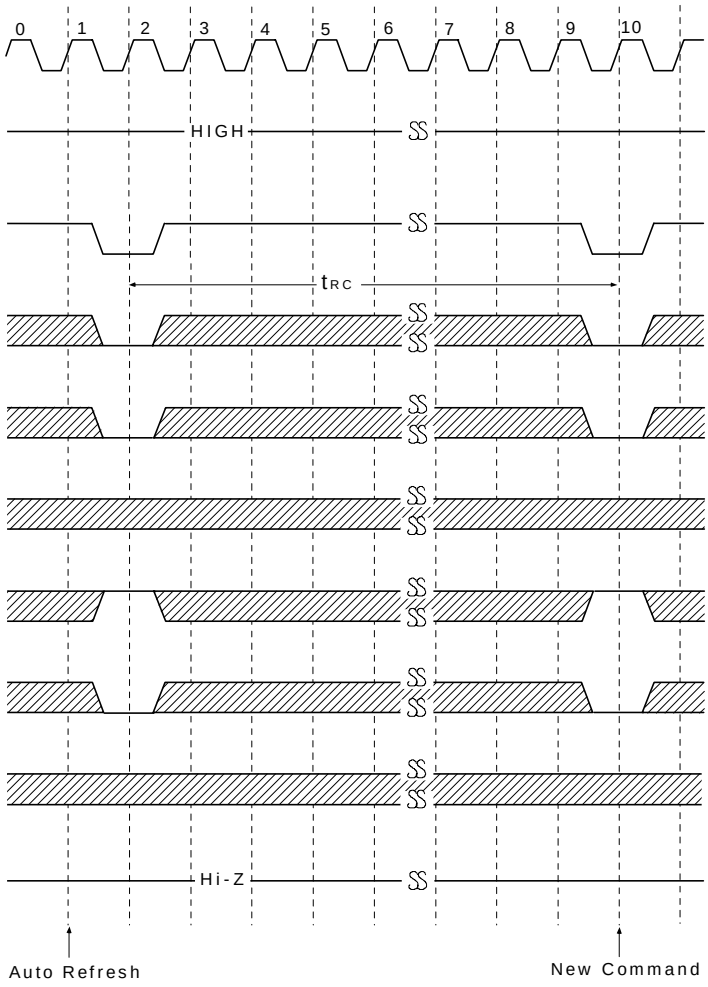
TO EXIT SELF REFRESH MODE

4. System clock restart and be stable before returning CKE high.
5. $\overline{CS}$ starts from high.
6. Minimum t_{RC} is required after CKE going high to complete self refresh exit.
7. 2K cycle of burst auto refresh is required before self refresh entry and after self refresh exit if the system uses burst refresh.

Mode Register Set Cycle



Auto Refresh Cycle



*Both bank precharge should be completed Mode Register Set cycle and auto refresh cycle.

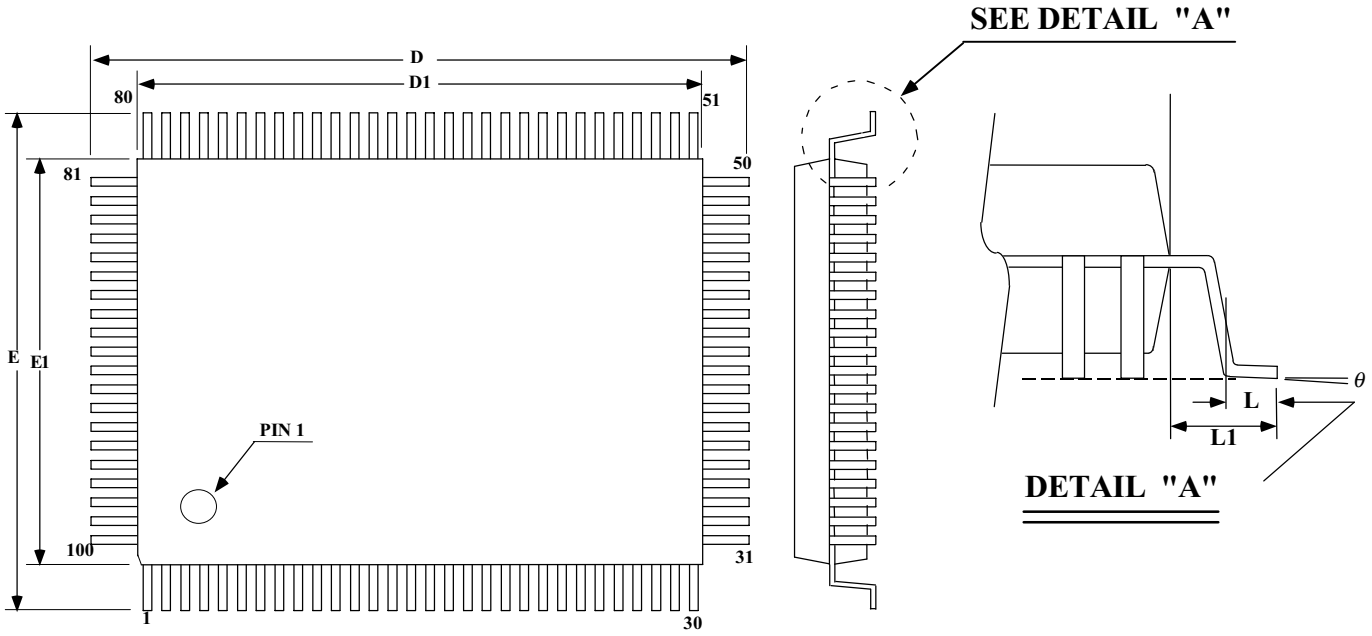
MODE REGISTER SET CYCLE

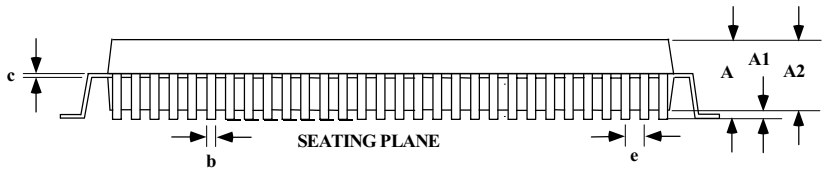
*Note : 1. $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ & $\overline{WE}$ activation and DSF of low at the same clock cycle with address key will set internal mode register.

2. Minimum 1 clock cycles should be met before new $\overline{RAS}$ activation.

3. Please refer to Mode Register Set table.

PACKING DIMENSIONS
100-LEAD QFP / TQFP (14 x 20 mm)





QFP							TQFP						
Symbol	Dimension in mm			Dimension in inch			Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max		Min	Norm	Max	Min	Norm	Max
A	___	___	3.400	___	___	0.134	A	___	___	1.20	___	___	0.047
A1	0.250	___	___	0.010	___	___	A1	0.05	___	___	0.002	___	___
A2	2.650	___	2.970	0.104	___	0.117	A2	0.95	___	1.00	0.037	___	0.039
b	0.220	___	0.380	0.0087	___	0.015	b	0.22	0.32	0.38	0.009	0.013	0.015
c	0.110	___	0.230	0.0043	___	0.009	c	0.09	___	0.20	0.035	___	0.008
D	23.000	23.200	23.400	0.906	0.913	0.921	D	22.95	23.20	23.45	0.904	0.913	0.923
D1	19.900	20.000	20.100	0.783	0.787	0.791	D1	19.90	20.00	20.10	0.783	0.787	0.791
E	17.000	17.200	17.400	0.669	0.677	0.685	E	16.95	17.20	17.45	0.667	0.677	0.687
E1	13.900	14.000	14.100	0.547	0.551	0.555	E1	13.90	14.00	14.10	0.547	0.551	0.555
L	0.650	0.800	0.950	0.026	0.031	0.037	L	0.65	0.80	0.95	0.026	0.031	0.037
L1	1.600 REF			0.063 REF			L1	1.60 REF			0.063 REF		
e	0.650 REF			0.026 REF			e	0.65 BSC			0.026 BSC		
θ	0°	___	7°	0°	___	7°	θ	0°	3.5°	7°	0°	3.5°	7°
y	___	___	0.080	___	___	0.003	y	___	___	0.08	___	___	0.003