

FSDH321, FSDL321

Green Mode Fairchild Power Switch (FPS™)

Features

- Internal Avalanche Rugged Sense FET
- Consumes only 0.65W at 240VAC & 0.3W load with Advanced Burst-Mode Operation
- Frequency Modulation for EMI Reduction
- Precision Fixed Operating Frequency
- Internal Start-up Circuit
- Pulse-by-Pulse Current Limiting
- Abnormal Over Current Protection (AOCP)
- Over Voltage Protection (OVP)
- Over Load Protection (OLP)
- Internal Thermal Shutdown Function (TSD)
- Auto-Restart Mode
- Under Voltage Lockout (UVLO)
- Low Operating Current (max 3mA)
- Adjustable Peak Current Limit
- Built-in Soft Start

Applications

- SMPS for STB, Low cost DVD Player
- Auxiliary Power for PC
- Adapter & Charger

Related Application Notes

- AN-4137, 4141, 4147(Flyback) / AN-4134(Forward)

Description

Each product in the FSDx321 (x for H, L) family consists of an integrated Pulse Width Modulator (PWM) and Sense FET, and is specifically designed for high performance off-line Switch Mode Power Supplies (SMPS) with minimal external components. Both devices are integrated high voltage power switching regulators which combine an avalanche rugged sense FET with a current mode PWM control block. The integrated PWM controller features include: a fixed oscillator with frequency modulation for reduced EMI, Under Voltage Lock Out (UVLO) protection, Leading Edge Blanking (LEB), an optimized gate turn-on/turn-off driver, Thermal Shut Down (TSD) protection, Abnormal Over Current Protection (AOCP) and temperature compensated precision current sources for loop compensation and fault protection circuitry. When compared to a discrete MOSFET and controller or RCC switching converter solution, the FSDx321 devices reduce total component count, design size, weight while increasing efficiency, productivity and system reliability. Both devices provide a basic platform that is well suited for the design of cost-effective flyback converters.

OUTPUT POWER TABLE

PRODUCT	230VAC $\pm 15\%$ ⁽³⁾		85-265VAC	
	Adapt-er ⁽¹⁾	Open Frame ⁽²⁾	Adapt-er ⁽¹⁾	Open Frame ⁽²⁾
FSDL321	11W	17W	8W	12W
FSDH321	11W	17W	8W	12W
FSDL0165RN	13W	23W	11W	17W
FSDM0265RN	16W	27W	13W	20W
FSDH0265RN	16W	27W	13W	20W
FSDL0365RN	19W	30W	16W	24W
FSDM0365RN	19W	30W	16W	24W
FSDL321L	11W	17W	8W	12W
FSDH321L	11W	17W	8W	12W
FSDL0165RL	13W	23W	11W	17W
FSDM0265RL	16W	27W	13W	20W
FSDH0265RL	16W	27W	13W	20W
FSDL0365RL	19W	30W	16W	24W
FSDM0365RL	19W	30W	16W	24W

Notes:

1. Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern as a heat sinker, at 50°C ambient.
2. Maximum practical continuous power in an open frame design with sufficient drain pattern as a heat sinker, at 50°C ambient.
3. 230 VAC or 100/115 VAC with doubler.

Typical Circuit

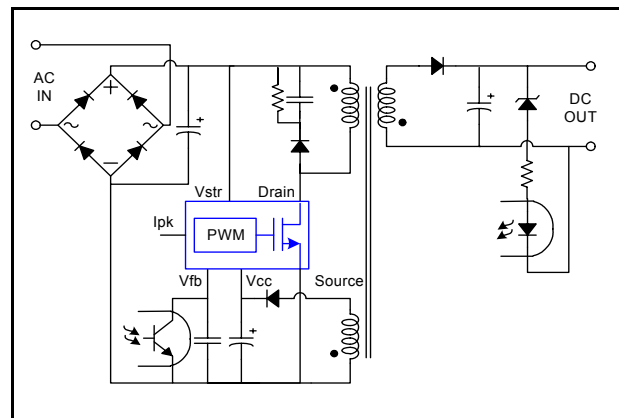


Figure 1. Typical Flyback Application

Internal Block Diagram

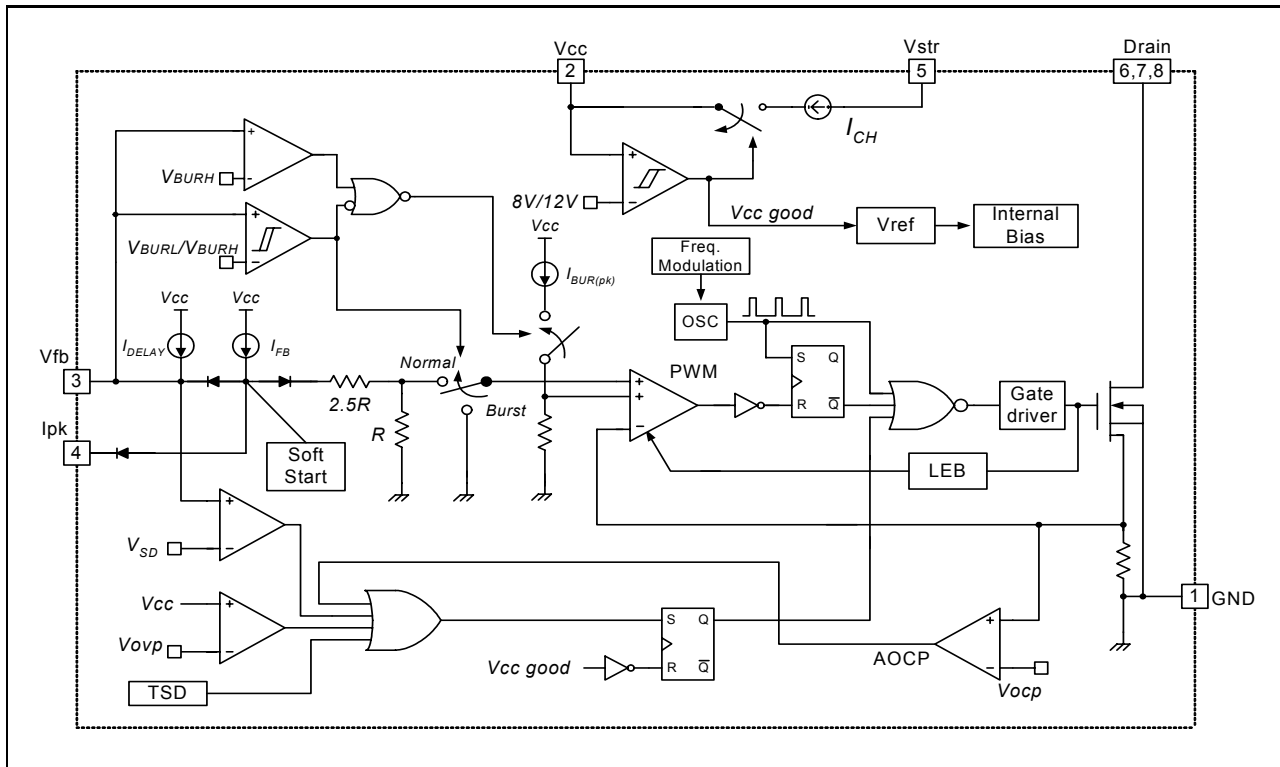


Figure 2. Functional Block Diagram of FSDx321

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	GND	Sense FET source terminal on primary side and internal control ground.
2	Vcc	Positive supply voltage input. Although connected to an auxiliary transformer winding, current is supplied from pin 5 (Vstr) via an internal switch during startup (see Internal Block Diagram section). It is not until Vcc reaches the UVLO upper threshold (12V) that the internal start-up switch opens and device power is supplied via the auxiliary transformer winding.
3	Vfb	The feedback voltage pin is the non-inverting input to the PWM comparator. It has a 0.9mA current source connected internally while a capacitor and optocoupler are typically connected externally. A feedback voltage of 6V triggers over load protection (OLP). There is a time delay while charging external capacitor Cfb from 3V to 6V using an internal 5uA current source. This time delay prevents false triggering under transient conditions, but still allows the protection mechanism to operate under true overload conditions.
4	l _{pk}	This pin adjusts the peak current limit of the Sense FET. The feedback 0.9mA current source is diverted to the parallel combination of an internal 2.8k Ω resistor and any external resistor to GND on this pin to determine the peak current limit. If this pin is tied to Vcc or left floating, the typical peak current limit will be 0.7A.
5	Vstr	This pin connects directly to the rectified AC line voltage source. At start up the internal switch supplies internal bias and charges an external storage capacitor placed between the Vcc pin and ground. Once the Vcc reaches 12V, the internal switch is opened.
6, 7, 8	Drain	The drain pins are designed to connect directly to the primary lead of the transformer and are capable of switching a maximum of 650V. Minimizing the length of the trace connecting these pins to the transformer will decrease leakage inductance.

Pin Configuration

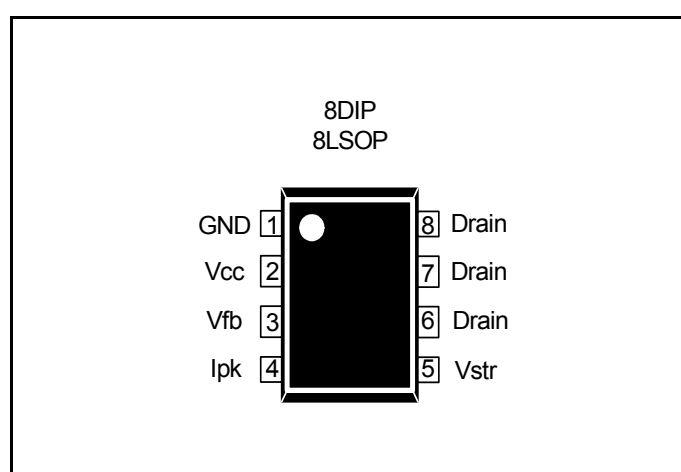


Figure 3. Pin Configuration (Top View)

Absolute Maximum Ratings

(Ta=25°C, unless otherwise specified)

Characteristic	Symbol	Value	Unit
Drain Pin Voltage	V _{DRAIN}	650	V
V _{str} Pin Voltage	V _{STR}	650	V
Drain-Gate Voltage	V _{DG}	650	V
Gate-Source Voltage	V _{GS}	± 20	V
Drain Current Pulsed ⁽¹⁾	I _{DM}	1.5	A
Continuous Drain Current (Tc=25°C)	I _D	0.7	A
Continuous Drain Current (Tc=100°C)	I _D	0.32	A
Single Pulsed Avalanche Energy ⁽²⁾	E _{AS}	10	mJ
Supply Voltage	V _{CC}	20	V
Feedback Voltage Range	V _{FB}	-0.3 to V _{CC}	V
Total Power Dissipation	P _D	1.40	W
Operating Junction Temperature	T _J	Internally limited	°C
Operating Ambient Temperature	T _A	-25 to +85	°C
Storage Temperature	T _{STG}	-55 to +150	°C

Note:

1. Repetitive rating: Pulse width is limited by maximum junction temperature
2. L = 24mH, starting T_J = 25°C

Thermal Impedance

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Value	Unit
8DIP			
Junction-to-Ambient Thermal ⁽¹⁾	θ _{JA}	88.84	°C/W
Junction-to-Case Thermal ⁽²⁾	θ _{JC}	13.94	°C/W

Note:

1. Free standing with no heatsink; Without copper clad.
/ Measurement Condition : Just before junction temperature T_J enters into OTP.
2. Measured on the DRAIN pin close to plastic interface.

- all items are tested with the standards JESD 51-2 and 51-10 (DIP).

Electrical Characteristics

(Ta = 25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SENSE FET SECTION						
Zero-Gate-Voltage Drain Current	IDSS	VDS=650V, VGS=0V	-	-	25	μA
		VDS=520V, VGS=0V, TC=125°C	-	-	200	
Drain-Source On-State Resistance	RDS(ON)	VGS=10V, ID=0.5A	-	14	19	Ω
Forward Trans-Conductance ⁽¹⁾	gfs	VDS=50V, ID=0.5A	1.0	1.3	-	S
Input Capacitance	CISS	VGS=0V, VDS=25V, f=1MHz	-	162	-	pF
Output Capacitance	COSS		-	18	-	
Reverse Transfer Capacitance	CRSS		-	3.8	-	
Turn-On Delay Time	td(on)	VDS=325V, ID=1.0A	-	9.5	-	ns
Rise Time	tr		-	19	-	
Turn-Off Delay Time	td(off)		-	33	-	
Fall Time	tf		-	42	-	
Total Gate Charge	Qg	VGS=10V, ID=1.0A, VDS=325V	-	7.0	-	nC
Gate-Source Charge	Qgs		-	3.1	-	
Gate-Drain (Miller) Charge	Qgd		-	0.4	-	
CONTROL SECTION						
Switching Frequency	fOSC	FSDH321	90	100	110	KHz
Switching Frequency Modulation	ΔfMOD		±2.5	±3.0	±3.5	KHz
Switching Frequency	fOSC	FSDL321	45	50	55	KHz
Switching Frequency Modulation	ΔfMOD		±1.0	±1.5	±2.0	KHz
Switching Frequency Variation ⁽²⁾	ΔfOSC	-25°C ≤ Ta ≤ 85°C	-	±5	±10	%
Maximum Duty Cycle	DMAX	FSDH321	62	67	72	%
		FSDL321	71	77	83	%
UVLO Threshold Voltage	VSTART	VFB=GND	11	12	13	V
	VSTOP	VFB=GND	7	8	9	V
Feedback Source Current	IFB	VFB=GND	0.7	0.9	1.1	mA
Internal Soft Start Time	ts/S	VFB=4V	10	15	20	ms
BURST MODE SECTION						
Burst Mode Voltage	VBURH	Tj=25°C	0.4	0.5	0.6	V
	VBURL		0.25	0.35	0.45	V
		VBUR(HYS)	Hysteresis	-	150	-
PROTECTION SECTION						
Peak Current Limit	ILIM	Tj=25°C, Δi/Δt=250mA/us	0.60	0.70	0.80	A
Current Limit Delay Time ⁽³⁾	tCLD	Tj=25°C	-	600	-	ns
Thermal Shutdown Temperature ⁽³⁾	TSD		125	145	-	°C
Shutdown Feedback Voltage	VSD		5.5	6.0	6.5	V
Over Voltage Protection	VOVP		18	19	20	V
Shutdown Delay Current	IDELAY	VFB=4V	3.5	5.0	6.5	μA
Leading Edge Blanking Time	tLEB		200	-	-	ns
TOTAL DEVICE SECTION						
Operating Supply Current (control part only)	IOP	VCC=14V, VFB=0V	1	3	5	mA
Start-Up Charging Current	ICH	VCC=0V	0.7	0.85	1.0	mA
Vstr Supply Voltage	VSTR	VCC=0V	35	-	-	V

Note:

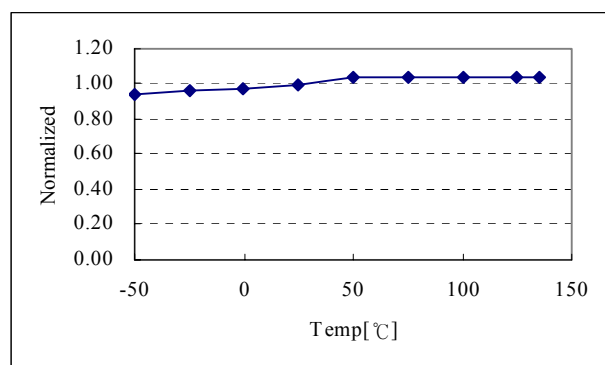
1. Pulse test: Pulse width ≤ 300us, duty ≤ 2%
2. These parameters, although guaranteed, are tested in EDS (wafer test) process
3. These parameters, although guaranteed, are not 100% tested in production

Comparison Between FSDM311 and FSDx321

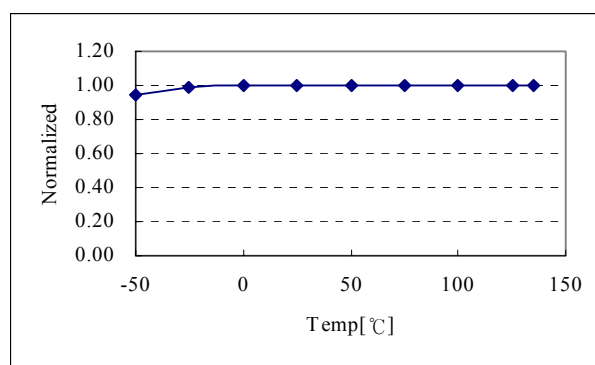
Function	FSDM311	FSDx321	FSDx321 Advantages
Soft-Start	15ms	15ms	(same for both devices) <ul style="list-style-type: none"> • Gradually increasing current limit during soft-start further reduces peak current and voltage stresses • Eliminates external components used for soft-start in most applications • Reduces or eliminates output overshoot
External Current Limit	not applicable	Programmable of default current limit	<ul style="list-style-type: none"> • Smaller transformer • Allows power limiting (constant over-load power) • Allows use of larger device for lower losses and higher efficiency.
Frequency Modulation	not applicable	$\pm 3.0\text{KHz}$ @100KHz $\pm 1.5\text{KHz}$ @50KHz	<ul style="list-style-type: none"> • Reduces conducted EMI
Burst Mode Operation	Built into controller	Built into controller	(same for both devices) <ul style="list-style-type: none"> • Improves light load efficiency • Reduces power consumption at no-load • Transformer audible noise reduction
Drain Creepage at Package	7.62mm	7.62mm	(same for both devices) <ul style="list-style-type: none"> • Greater immunity to arcing provoked by dust, debris and other contaminants

Typical Performance Characteristics (Control Part)

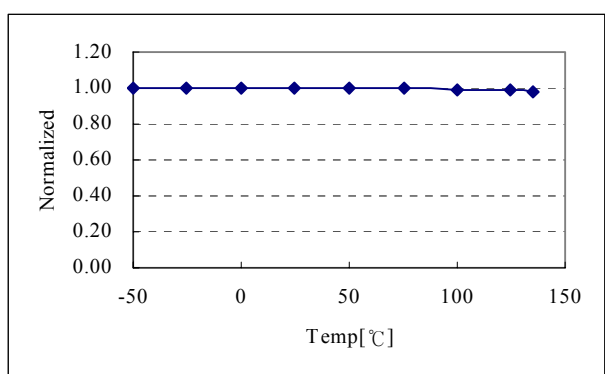
(These characteristic graphs are normalized at $T_a = 25^\circ\text{C}$)



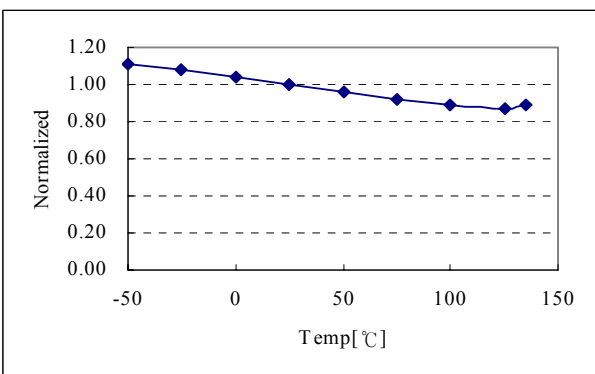
Operating Frequency (Fosc) vs. Ta



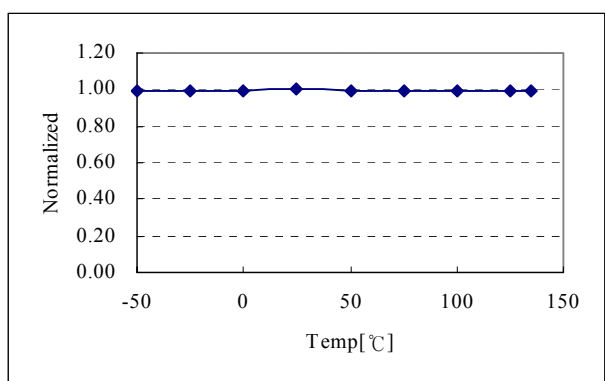
Frequency Modulation (ΔF_{mod}) vs. Ta



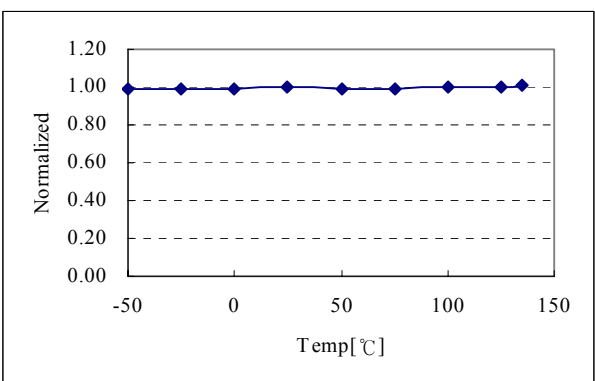
Maximum Duty Cycle (Dmax) vs. Ta



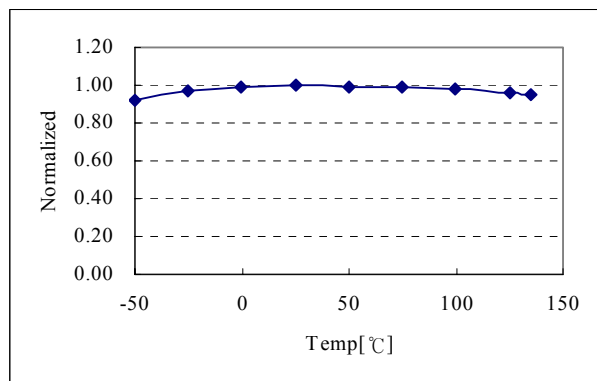
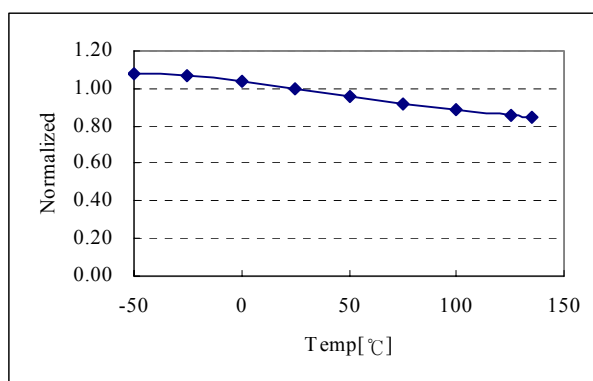
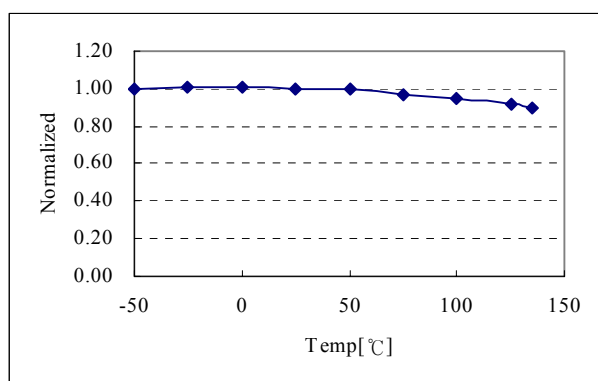
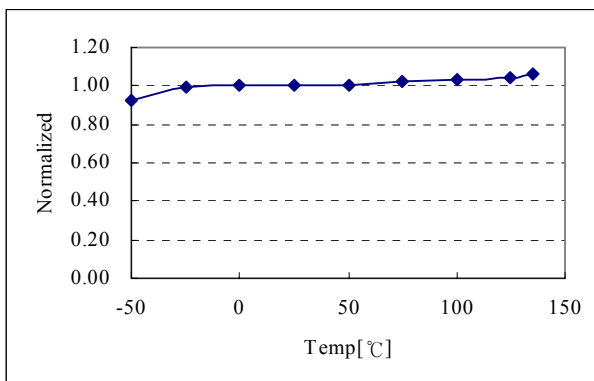
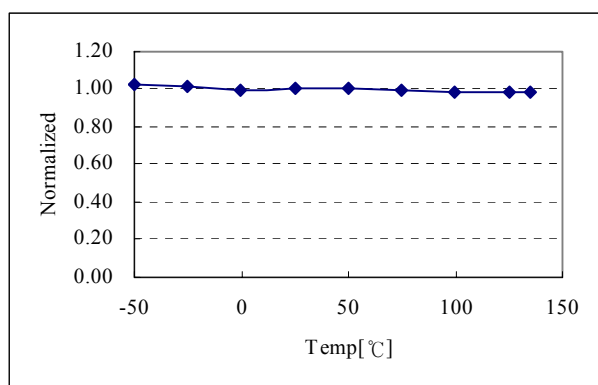
Operating Supply Current (IOP) vs. Ta



Start Threshold Voltage (VSTART) vs. Ta



Stop Threshold Voltage (VSTOP) vs. Ta

Typical Performance Characteristics (Continued)**Feedback Source Current (I_{FB}) vs. T_a** **Start Up Charging Current (I_{CH}) vs. T_a** **Peak Current Limit (I_{LIM}) vs. T_a** **Burst Peak Current ($I_{BUR(pk)}$) vs. T_a** **Over Voltage Protection (V_{OVP}) vs. T_a**

Functional Description

1. Startup : In previous generations of Fairchild Power Switches (FPS™) the Vstr pin had an external resistor to the DC input voltage line. In this generation the startup resistor is replaced by an internal high voltage current source and a switch that shuts off when 15ms goes by after the supply voltage, Vcc, gets above 12V. The source turns back on if Vcc drops below 8V.

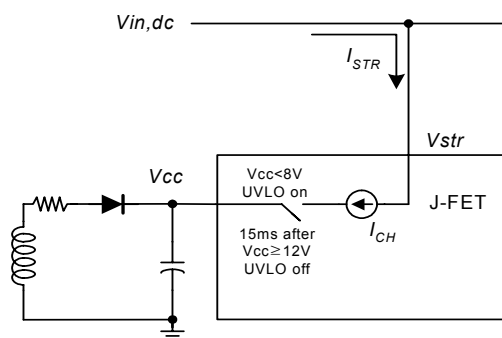


Figure 4. High Voltage Current Source

2. Feedback Control : The FSDx321 employs current mode control, as shown in Figure 5. An opto-coupler (such as the H11A817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the Rsense resistor plus an offset voltage makes it possible to control the switching duty cycle. When the KA431 reference pin voltage exceeds the internal reference voltage of 2.5V, the opto-coupler LED current increases, the feedback voltage Vfb is pulled down and it reduces the duty cycle. This event typically happens when the input voltage is increased or the output load is decreased.

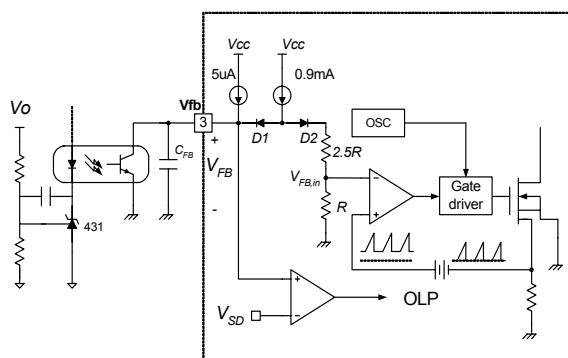


Figure 5. Pulse Width Modulation (PWM) Circuit

3. Leading Edge Blanking (LEB) : At the instant the internal Sense FET is turned on, the primary side capacitance and secondary side rectifier diode reverse recovery typically cause a high current spike through the Sense FET. Excessive voltage across the Rsense resistor leads to incorrect feedback operation in the current mode PWM control. To counter this effect, the FPS employs a leading edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (t_{LEB}) after the Sense FET is turned on.

4. Protection Circuits : The FPS has several protective functions such as over load protection (OLP), over voltage protection (OVP), abnormal over current protection (AOCP), under voltage lock out (UVLO) and thermal shut-down (TSD). Because these protection circuits are fully integrated inside the IC without external components, the reliability is improved without increasing cost. Once a fault condition occurs, switching is terminated and the Sense FET remains off. This causes Vcc to fall. When Vcc reaches the UVLO stop voltage VSTOP (8V), the protection is reset and the internal high voltage current source charges the Vcc capacitor via the Vstr pin. When Vcc reaches the UVLO start voltage VSTART (12V), the FPS resumes its normal operation. In this manner, the auto-restart can alternately enable and disable the switching of the power Sense FET until the fault condition is eliminated.

4.1 Over Load Protection (OLP) : Overload is defined as the load current exceeding a pre-set level due to an unexpected event. In this situation, the protection circuit should be activated in order to protect the SMPS. However, even when the SMPS is operating normally, the over load protection (OLP) circuit can be activated during the load transition. In order to avoid this undesired operation, the OLP circuit is designed to be activated after a specified time to determine whether it is a transient situation or an overload situation. In conjunction with the Ipk current limit pin (if used) the current mode feedback path would limit the current in the Sense FET when the maximum PWM duty cycle is attained. If the output consumes more than this maximum power, the output voltage (V_o) decreases below its rating voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (VFB). If VFB exceeds 3V, the feedback input diode is blocked and the 5uA current source (IDE-LAY) starts to charge Cfb slowly up to Vcc. In this condition, VFB increases until it reaches 6V, when the switching operation is terminated as shown in Figure 6. The shutdown delay time is the time required to charge Cfb from 3V to 6V with 5uA current source.

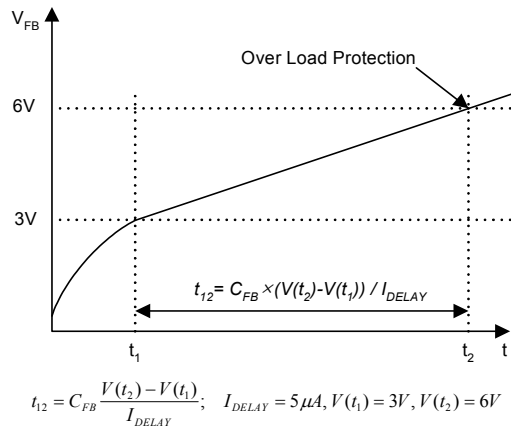


Figure 6. Over Load Protection (OLP)

4.2 Thermal Shutdown (TSD) : The Sense FET and the control IC are integrated, making it easier for the control IC to detect the temperature of the Sense FET. When the temperature exceeds approximately 145°C, thermal shutdown is activated.

4.3 Abnormal Over Current Protection (AOCP) : Even though the FPS has OLP (Over Load Protection) and current mode PWM feedback, these are not enough to protect the FPS when a secondary side diode short or a transformer pin short occurs. In addition to start-up, soft-start is also activated at each restart attempt during auto-restart and when restarting after latch mode is activated. The FPS has an internal AOCP (Abnormal Over Current Protection) circuit, as shown in Figure 7. When the gate turn-on signal is applied to the power Sense FET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is then compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, pulse-by-pulse AOCP is triggered regardless of uncontrollable LEB time. Here, pulse-by-pulse AOCP stops the Sense FET within 350ns after it is activated.

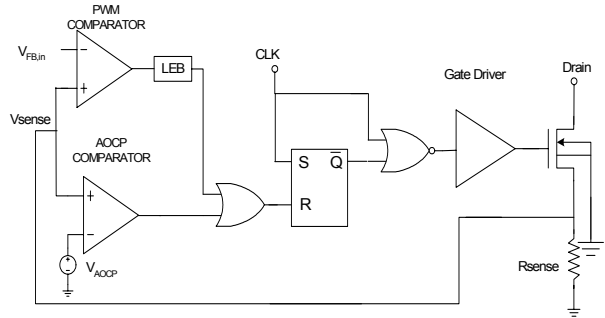


Figure 7. Abnormal Over Current Protection (AOCP)

4.4 Over Voltage Protection (OVP) : In the event of a malfunction in the secondary side feedback circuit, or an open feedback loop caused by a soldering defect, the current through the opto-coupler transistor becomes almost zero (refer to Figure 5). Then, V_FB climbs up in a similar manner to the over load situation, forcing the preset maximum current to be supplied to the SMPS until the over load protection is activated. Because excess energy is provided to the output, the output voltage may exceed the rated voltage before the over load protection is activated, resulting in the breakdown of the devices in the secondary side. In order to prevent this situation, an over voltage protection (OVP) circuit is employed. In general, V_{CC} is proportional to the output voltage and the FPS uses V_{CC} instead of directly monitoring the output voltage. If V_{CC} exceeds 19V, OVP circuit is activated resulting in termination of the switching operation. In order to avoid undesired activation of OVP during normal operation, V_{CC} should be properly designed to be below 19V.

5. Soft Start : The FPS has an internal soft start circuit that slowly increases the feedback voltage together with the Sense FET current after it starts up. The typical soft start time is 15msec, as shown in Figure 8, where progressive increments of the Sense FET current are allowed during the start-up phase. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. It also helps to prevent transformer saturation and reduce the stress on the secondary diode.

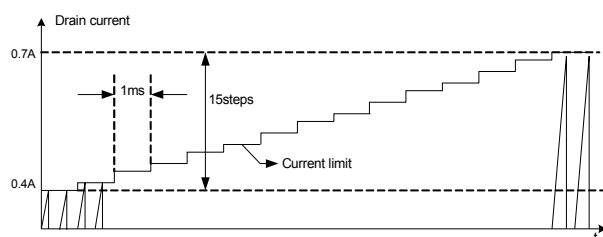


Figure 8. Soft Start Function

6. Burst Operation : In order to minimize power dissipation in standby mode, the FPS enters burst mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 9, the device automatically enters burst mode when the feedback voltage drops below V_{BURH} (500mV). Switching still continues but the current limit is set to a fixed limit internally to minimize flux density in the transformer. The fixed current limit is larger than that defined by $V_{FB} = V_{BURH}$ and therefore, V_{FB} is driven down further. Switching continues until the feedback voltage drops below V_{BURL} (350mV). At this point switching stops and the output voltages start to drop at a rate dependent on the standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (500mV), switching resumes. The feedback voltage then falls and the process repeats. Burst mode operation alternately enables and disables switching of the power Sense FET thereby reducing switching loss in Standby mode.

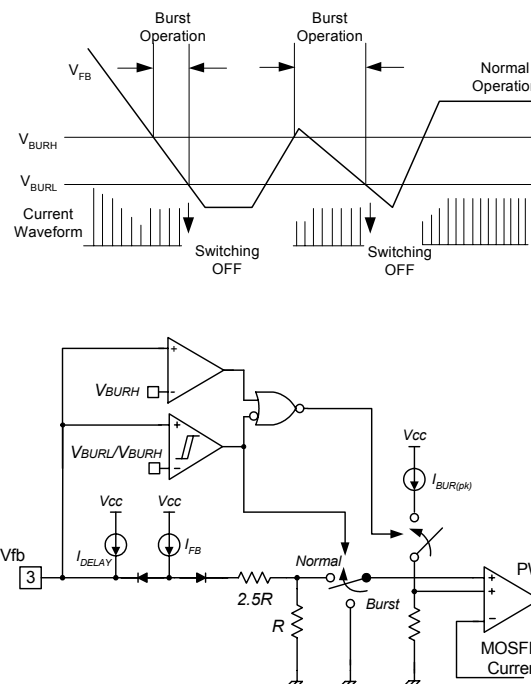


Figure 9. Burst Operation Function

7. Frequency Modulation : Modulating the switching frequency of a switched power supply can reduce EMI. Frequency modulation can reduce EMI by spreading the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. The amount of EMI reduction is directly related to the depth of the reference frequency. As can be seen in Figure 10, the frequency changes from 97KHz to 103KHz in 4ms for the FSDH321 (48.5KHz to 51.5KHz for FSDL321). Frequency modulation allows the use of a cost effective inductor instead of an AC input mode choke to satisfy the requirements of world wide EMI limits.

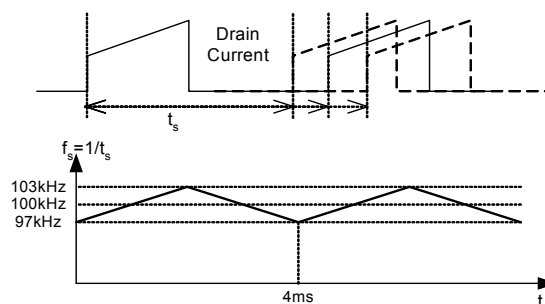


Figure 10. Frequency Modulation Waveform

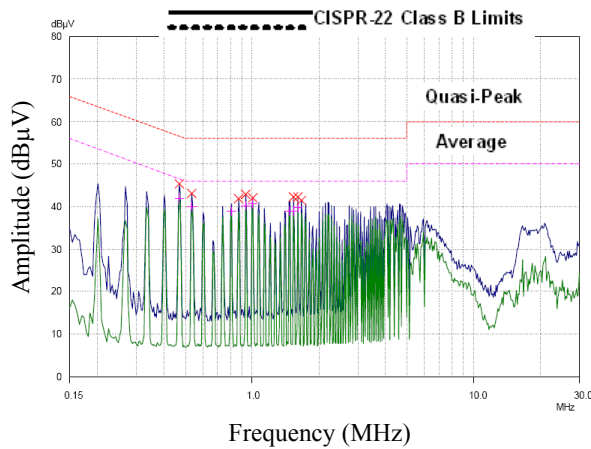


Figure 11. KA5-series FPS Full Range EMI scan(67KHz, no Frequency Modulation) with DVD Player SET

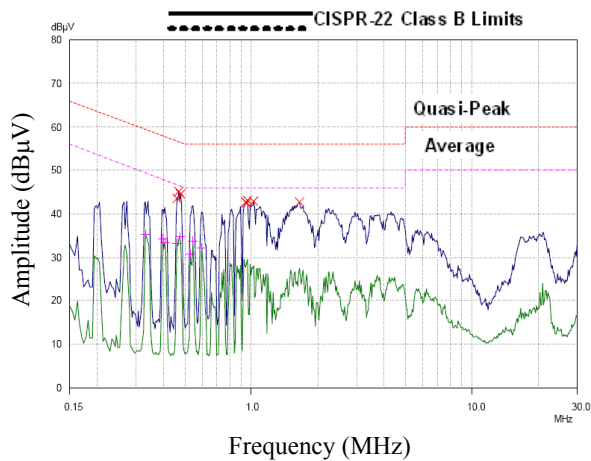


Figure 12. FSDX-series FPS Full Range EMI Scan (67KHz, with Frequency Modulation) with DVD Player SET

8. Adjusting Peak Current Limit : As shown in Figure 13, a combined $2.8\text{k}\Omega$ internal resistance is connected to the non-inverting lead on the PWM comparator. A external resistance of Rx on the current limit pin forms a parallel resistance with the $2.8\text{k}\Omega$ when the internal diodes are biased by the main current source of $900\mu\text{A}$.

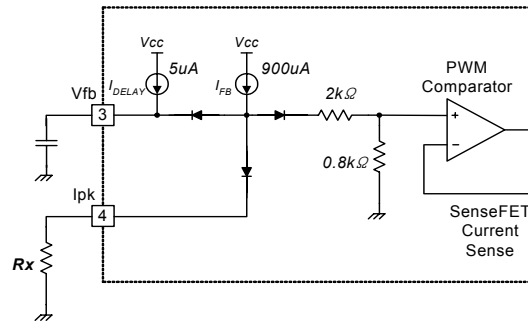


Figure 13. Peak Current Limit Adjustment

For example, FSDx321 has a typical Sense FET peak current limit (I_{LIM}) of 0.7A . I_{LIM} can be adjusted to 0.5A by inserting Rx between the Ipk pin and the ground. The value of the Rx can be estimated by the following equations:

$$0.7\text{A} : 0.5\text{A} = 2.8\text{k}\Omega : X\text{k}\Omega ,$$

$$X = R_x \parallel 2.8\text{k}\Omega .$$

(X represents the resistance of the parallel network)

Typical Application Circuit

Application	Output power	Input voltage	Output voltage (Max current)
PC Auxiliary Power Supply	10W	DC 140~375V	5.0V (2.0A)

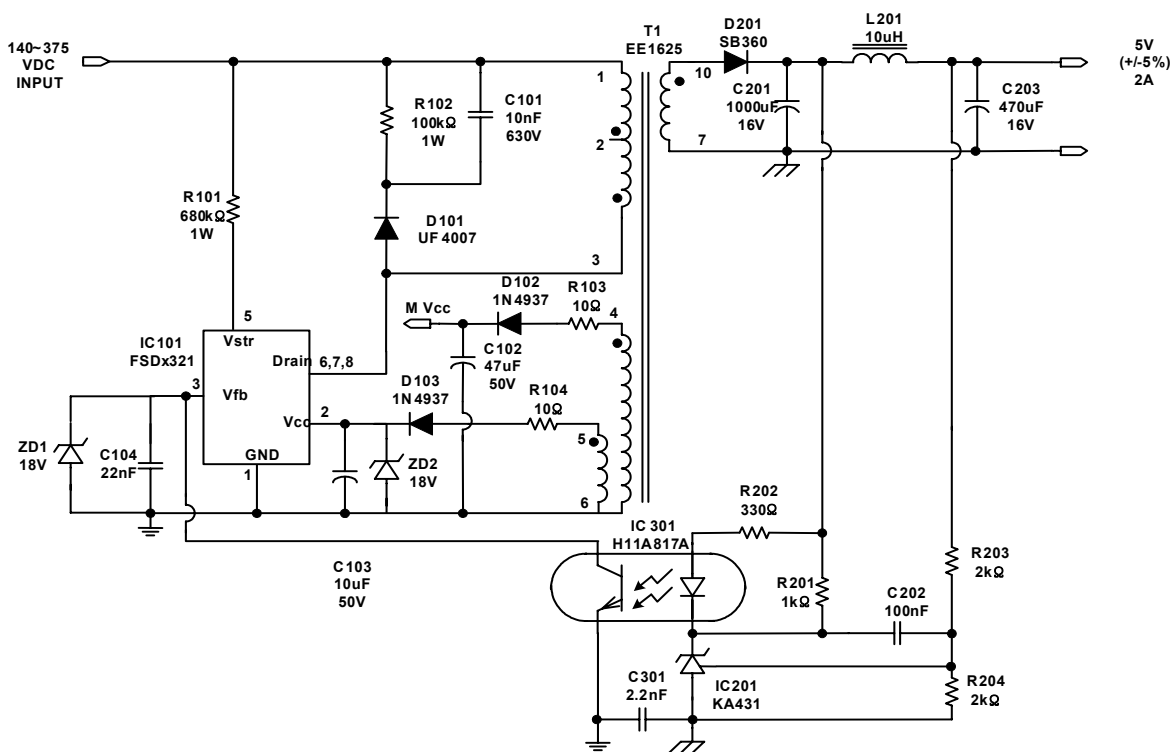
Features

- High efficiency (>70% at full load, full input range)
- Low standby mode power consumption (<1W at DC 375V input and 0.5W load)
- Low component count
- Enhanced system reliability through various protection functions
- Low EMI through frequency modulation
- Internal soft-start (15ms)

Key Design Notes

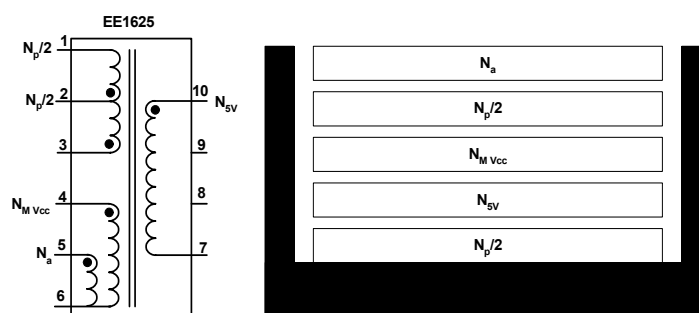
- The delay time for over load protection is designed to be about 13ms with C104 of 22nF. If faster/slower triggering of OLP is required, C104 can be changed to a smaller/larger value(eg. 47nF for about 30ms).
- The pulse-by-pulse peak current limit level(I_{LIM}) is set to default value 0.7A by floating the Ipk pin (#4).
- R102 and C101 clamp the DRAIN voltage of MOSFET below 650V under all conditions.

1. Schematic



10W PC Auxiliary Power Circuit

2. Transformer Schematic Diagram



3. Winding Specification

	Pin(S → F)	Wire	Turns	Winding Method
$N_p/2$	3 → 2	0.15 ϕ × 1	80	Solenoid winding
Insulation : Polyester Tape t = 0.050mm, 3Layers				
N_{SV}	10 → 7	0.55 ϕ × 1	12	Solenoid winding
Insulation : Polyester Tape t = 0.050mm, 3Layers				
$N_{M Vcc}$	4 → 6	0.20 ϕ × 1	40	Solenoid winding
Insulation : Polyester Tape t = 0.050mm, 3Layers				
$N_{P/2}$	2 → 1	0.15 ϕ × 1	80	Solenoid winding
Insulation : Polyester Tape t = 0.050mm, 3Layers				
N_a	5 → 6	0.20 ϕ × 1	34	Solenoid winding
Outer Insulation : Polyester Tape t = 0.050mm, 3Layers				

4. Electrical Characteristics

	Pin	Spec.	Remark
Inductance	1 - 3	1.8 mH	1kHz, 1V
Leakage	1 - 3	100 uH	2nd side all short

5. Core & Bobbin

Core : EER1625

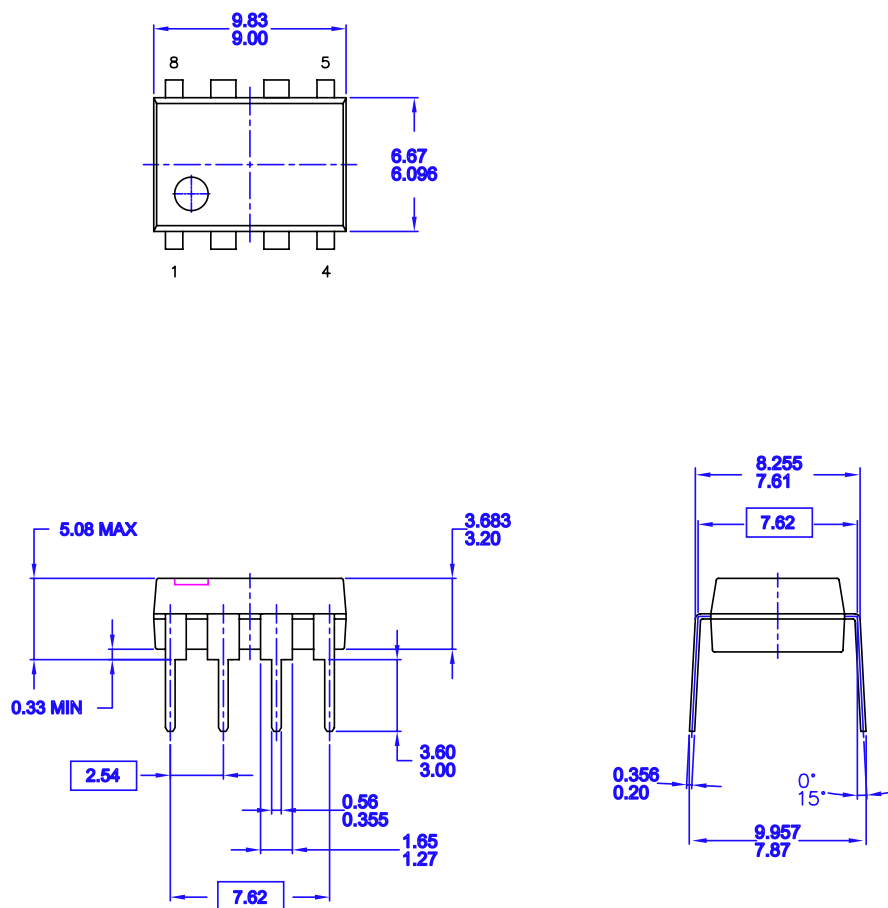
Bobbin : EER1625

6. Demo Circuit Part List

Part	Value	Note	Part	Value	Note
Resistor			Inductor		
R101	680K	1W	L201	10uH	-
R102	100K	1W			-
R103	10	1/4W	Diode		
R104	10	1/4W	D101	UF4007	PN Ultra Fast
R201	1K	1/4W	D102	1N4937	PN Ultra Fast
R202	330	1/4W	D103	1N4937	PN Ultra Fast
R203	2K	1/4W	D201	SB360	Schottky
R204	2K	1/4W	ZD1	1N4746A	18V Zener
			ZD2	1N4746A	18V Zener
Capacitor			IC		
C101	10nF/630V	Film			
C102	47uF/50V	Electrolytic	IC101	FSDH321	FPS™
C103	10uF/50V	Electrolytic	IC201	KA431(TL431)	Voltage reference
C104	22nF/50V	Film	IC301	H11A817A	Opto-Coupler
C201	1000uF/16V	Electrolytic			
C202	100nF/50V	Ceramic			
C203	1uF/100V	Electrolytic			
C204	470uF/16V	Electrolytic			
C301	2.2nF/35V	Ceramic			

Package Dimensions

8DIP

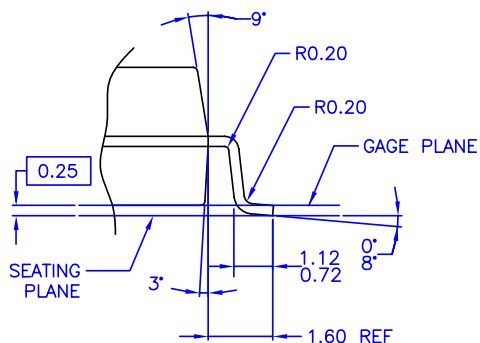
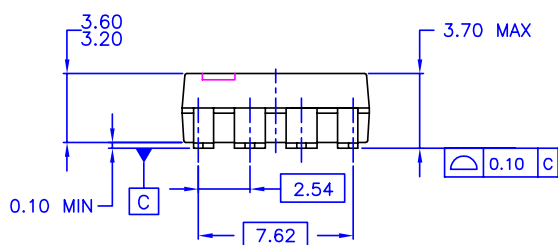
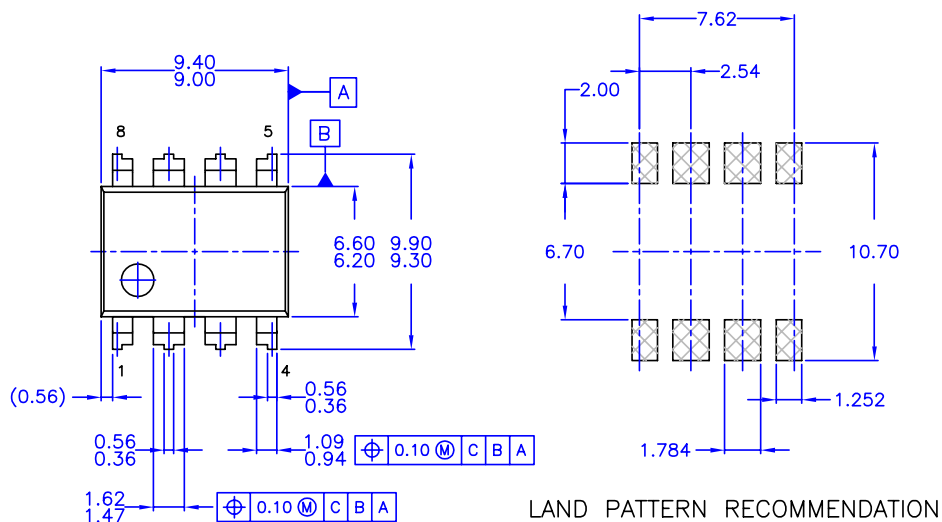


NOTES: UNLESS OTHERWISE SPECIFIED
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 B) ALL DIMENSIONS ARE IN MILLIMETERS.
 C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
 D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

MKT-N08FrevB

Package Dimensions (Continued)

8LSOP



- NOTES: UNLESS OTHERWISE SPECIFIED
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 - ALL DIMENSIONS ARE IN MILLIMETERS.
 - DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
 - DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

DETAIL A
SCALE: 2X

Ordering Information

Product Number	Package	Marking Code	BVdss	fosc	RDS(ON)
FSDH321	8DIP	DH321	650V	100KHz	14Ω
FSDL321	8DIP	DL321	650V	50KHz	14Ω
FSDH321L	8LSOP	DH321	650V	100KHz	14Ω
FSDL321L	8LSOP	DL321	650V	50KHz	14Ω

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