
HM628512C Series

4 M SRAM (512-kword \times 8-bit)

HITACHI

ADE-203-1212 (Z)
Preliminary
Rev. 0.0
Sep. 12, 2000

Description

The Hitachi HM628512C is a 4-Mbit static RAM organized 512-kword \times 8-bit. It realizes higher density, higher performance and low power consumption by employing Hi-CMOS process technology. The device, packaged in a 525-mil SOP (foot print pitch width) or 400-mil TSOP TYPE II or 600-mil plastic DIP, is available for high density mounting. The HM628512C is suitable for battery backup system.

Features

- Single 5 V supply
- Access time: 55/70 ns (max)
- Power dissipation
 - Active: 50 mW/MHz (typ)
 - Standby: 10 μ W (typ)
- Completely static memory. No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Battery backup operation

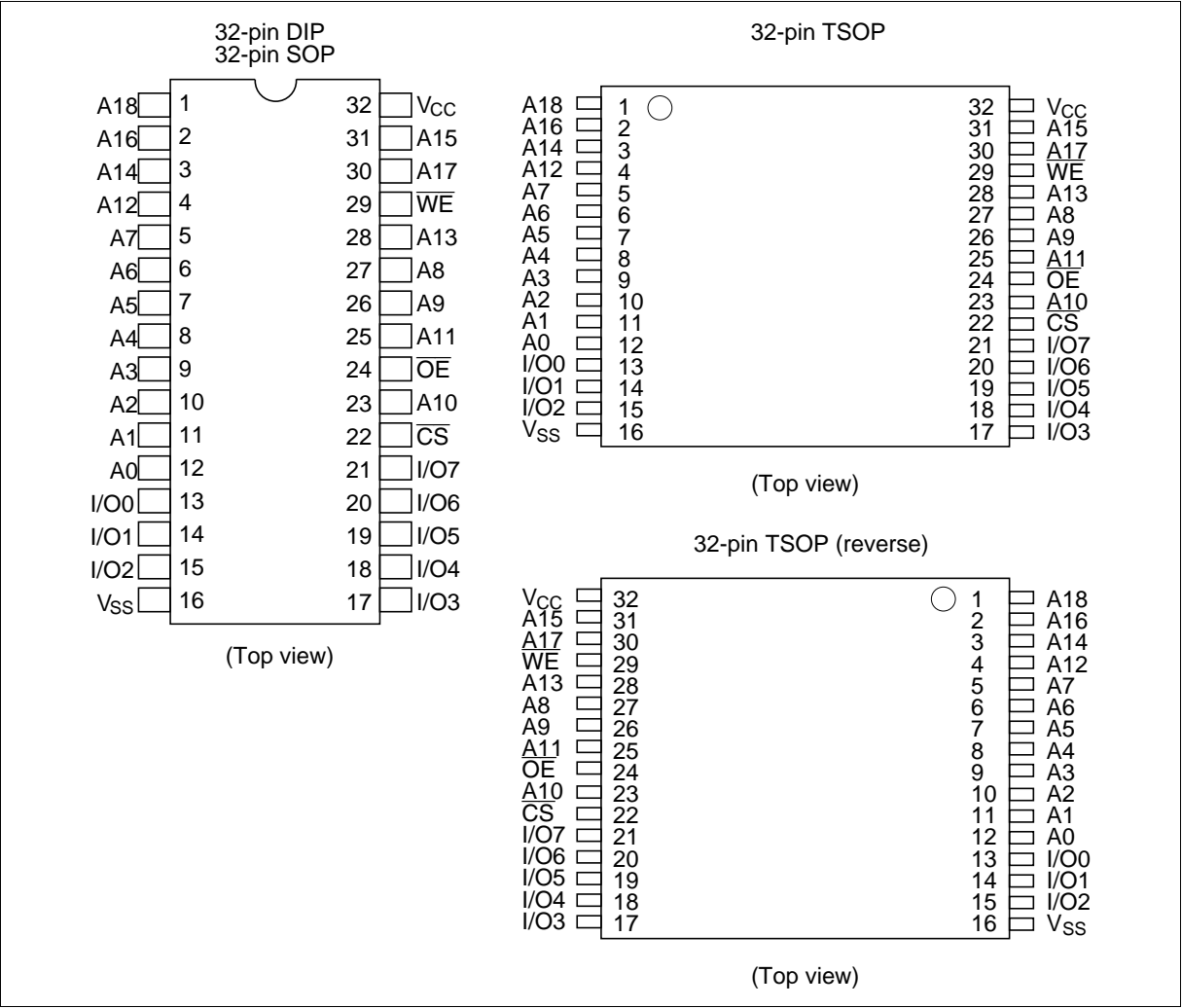
Preliminary: The specification of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specification.

HM628512C Series

Ordering Information

Type No.	Access time	Package
HM628512CLP-5	55 ns	600-mil 32-pin plastic DIP (DP-32)
HM628512CLP-7	70 ns	
HM628512CLP-5SL	55 ns	525-mil 32-pin plastic SOP (FP-32D)
HM628512CLP-7SL	70 ns	
HM628512CLFP-5	55 ns	400-mil 32-pin plastic TSOP II (TTP-32D)
HM628512CLFP-7	70 ns	
HM628512CLFP-5SL	55 ns	400-mil 32-pin plastic TSOP II reverse (TTP-32DR)
HM628512CLFP-7SL	70 ns	
HM628512CLTT-5	55 ns	400-mil 32-pin plastic TSOP II (TTP-32D)
HM628512CLTT-7	70 ns	
HM628512CLTT-5SL	55 ns	400-mil 32-pin plastic TSOP II reverse (TTP-32DR)
HM628512CLTT-7SL	70 ns	
HM628512CLRR-5	55 ns	400-mil 32-pin plastic TSOP II reverse (TTP-32DR)
HM628512CLRR-7	70 ns	
HM628512CLRR-5SL	55 ns	400-mil 32-pin plastic TSOP II reverse (TTP-32DR)
HM628512CLRR-7SL	70 ns	

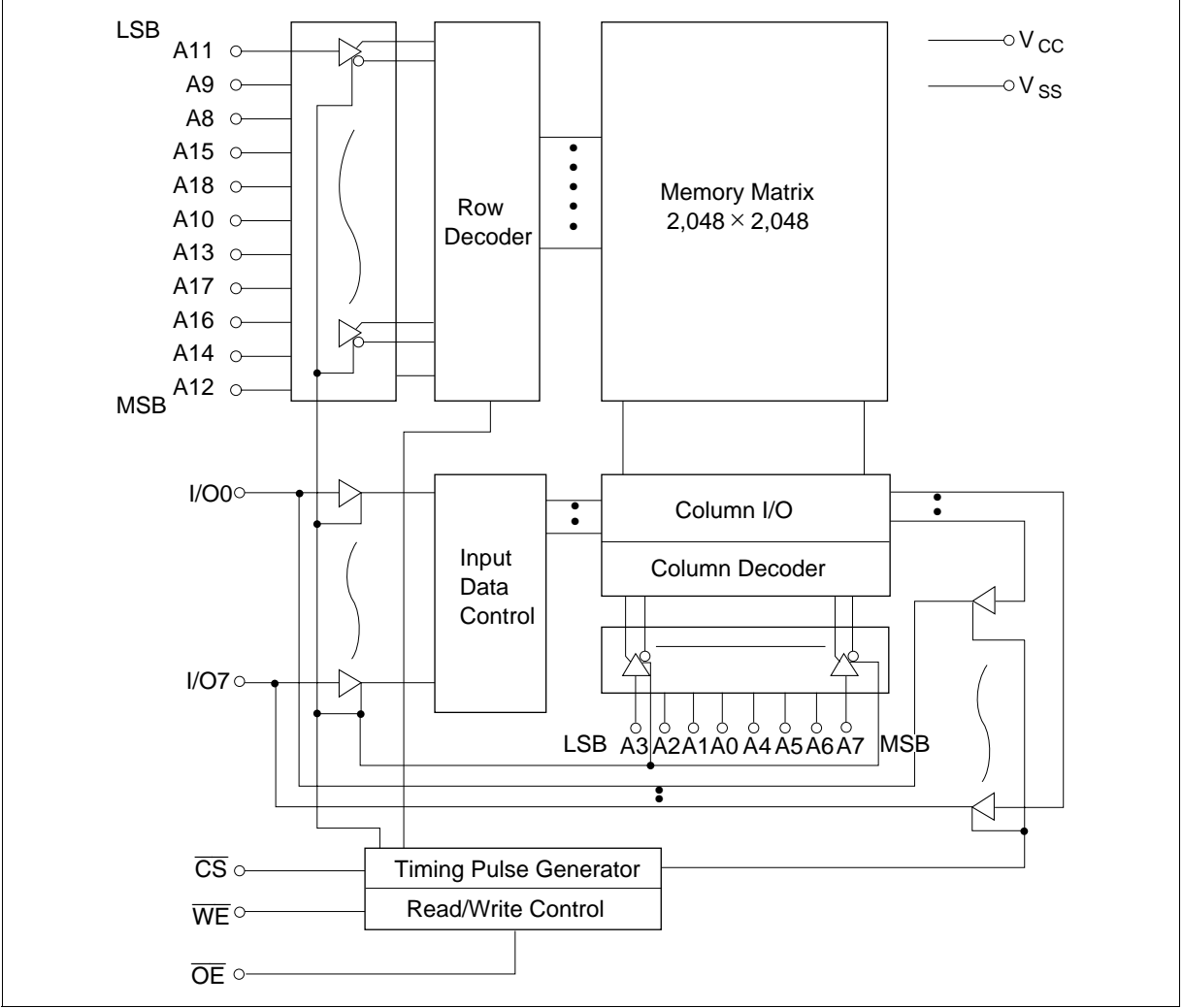
Pin Arrangement



Pin Description

Pin name	Function
A0 to A18	Address input
I/O0 to I/O7	Data input/output
\overline{CS}	Chip select
\overline{OE}	Output enable
\overline{WE}	Write enable
V _{CC}	Power supply
V _{SS}	Ground

Block Diagram



Function Table

$\overline{\text{WE}}$	$\overline{\text{CS}}$	$\overline{\text{OE}}$	Mode	V_{CC} current	Dout pin	Ref. cycle
×	H	×	Not selected	$I_{\text{SB}}, I_{\text{SB1}}$	High-Z	—
H	L	H	Output disable	I_{CC}	High-Z	—
H	L	L	Read	I_{CC}	Dout	Read cycle
L	L	H	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: ×: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage	V_{CC}	−0.5 to +7.0	V
Voltage on any pin relative to V_{SS}	V_{T}	−0.5* ¹ to $V_{\text{CC}} + 0.3$ * ²	V
Power dissipation	P_{T}	1.0	W
Operating temperature	T_{opr}	−20 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C
Storage temperature under bias	T_{bias}	−20 to +85	°C

Notes: 1. V_{T} min: −3.0 V for pulse half-width ≤ 30 ns.

2. Maximum voltage is 7.0 V.

Recommended DC Operating Conditions ($T_{\text{a}} = -20$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.2	—	$V_{\text{CC}} + 0.3$	V
Input low voltage	V_{IL}	−0.3* ¹	—	0.8	V

Note: 1. V_{IL} min: −3.0 V for pulse half-width ≤ 30 ns.

DC Characteristics (Ta = -20 to +70°C, V_{CC} = 5 V ±10% , V_{SS} = 0 V)

Parameter	Symbol	Min	Typ* ¹	Max	Unit	Test conditions
Input leakage current	I _{LI}	—	—	1	μA	V _{in} = V _{SS} to V _{CC}
Output leakage current	I _{LO}	—	—	1	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, V _{I/O} = V _{SS} to V _{CC}
Operating power supply current: DC	I _{CC}	—	8	15	mA	$\overline{CS} = V_{IL}$, others = V _{IH} /V _{IL} , I _{I/O} = 0 mA
Operating power supply current	I _{CC1}	—	40	60	mA	Min cycle, duty = 100% $\overline{CS} = V_{IL}$, others = V _{IH} /V _{IL} I _{I/O} = 0 mA
Operating power supply current	I _{CC2}	—	10	20	mA	Cycle time = 1 μs, duty = 100% I _{I/O} = 0 mA, $\overline{CS} \leq 0.2$ V V _{IH} ≥ V _{CC} - 0.2 V, V _{IL} ≤ 0.2 V
Standby power supply current: DC	I _{SB}	—	1	3	mA	$\overline{CS} = V_{IH}$
Standby power supply current (1): DC	I _{SB1}	—	2* ²	100* ²	μA	V _{in} ≥ 0 V, $\overline{CS} \geq V_{CC} - 0.2$ V
		—	2* ³	50* ³	μA	
Output low voltage	V _{OL}	—	—	0.4	V	I _{OL} = 2.1 mA
Output high voltage	V _{OH}	2.4	—	—	V	I _{OH} = -1.0 mA

- Notes: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and specified loading, and not guaranteed.
2. This characteristics is guaranteed only for L version.
3. This characteristics is guaranteed only for L-SL version.

Capacitance (Ta = +25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit	Test conditions
Input capacitance* ¹	C _{in}	—	8	pF	V _{in} = 0 V
Input/output capacitance* ¹	C _{I/O}	—	10	pF	V _{I/O} = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics ($T_a = -20$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.8 V to 2.4 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate + C_L (100 pF) (HM628512C-7)
1 TTL Gate + C_L (50 pF) (HM628512C-5)
(Including scope & jig)

Read Cycle

		HM628512C					
		-5		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t _{RC}	55	—	70	—	ns	
Address access time	t _{AA}	—	55	—	70	ns	
Chip select access time	t _{CO}	—	55	—	70	ns	
Output enable to output valid	t _{OE}	—	25	—	35	ns	
Chip selection to output in low-Z	t _{LZ}	10	—	10	—	ns	2
Output enable to output in low-Z	t _{OLZ}	5	—	5	—	ns	2
Chip deselection to output in high-Z	t _{HZ}	0	20	0	25	ns	1, 2
Output disable to output in high-Z	t _{OHZ}	0	20	0	25	ns	1, 2
Output hold from address change	t _{OH}	10	—	10	—	ns	

Write Cycle

		HM628512C					
		-5		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write cycle time	t _{WC}	55	—	70	—	ns	
Chip selection to end of write	t _{CW}	50	—	60	—	ns	4
Address setup time	t _{AS}	0	—	0	—	ns	5
Address valid to end of write	t _{AW}	50	—	60	—	ns	
Write pulse width	t _{WP}	40	—	50	—	ns	3, 12
Write recovery time	t _{WR}	0	—	0	—	ns	6
\overline{WE} to output in high-Z	t _{WHZ}	0	20	0	25	ns	1, 2, 7
Data to write time overlap	t _{DW}	25	—	30	—	ns	
Data hold from write time	t _{DH}	0	—	0	—	ns	
Output active from output in high-Z	t _{OW}	5	—	5	—	ns	2
Output disable to output in high-Z	t _{OHZ}	0	20	0	25	ns	1, 2, 7

Notes: 1. t_{HZ} , t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

2. This parameter is sampled and not 100% tested.

3. A write occurs during the overlap (t_{WP}) of a low \overline{CS} and a low \overline{WE} . A write begins at the later transition of \overline{CS} going low or \overline{WE} going low. A write ends at the earlier transition of \overline{CS} going high or \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.

4. t_{CW} is measured from \overline{CS} going low to the end of write.

5. t_{AS} is measured from the address valid to the beginning of write.

6. t_{WR} is measured from the earlier of \overline{WE} or \overline{CS} going high to the end of write cycle.

7. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.

8. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} transition, the output remain in a high impedance state.

9. Dout is the same phase of the write data of this write cycle.

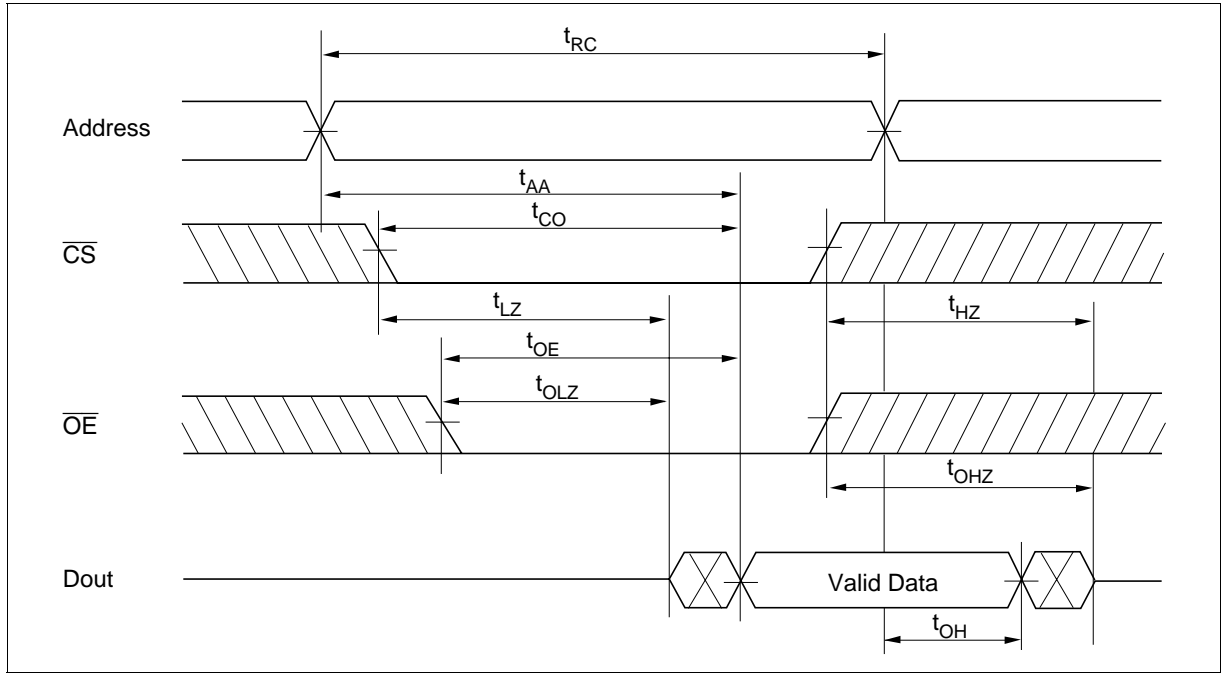
10. Dout is the read data of next address.

11. If \overline{CS} is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.

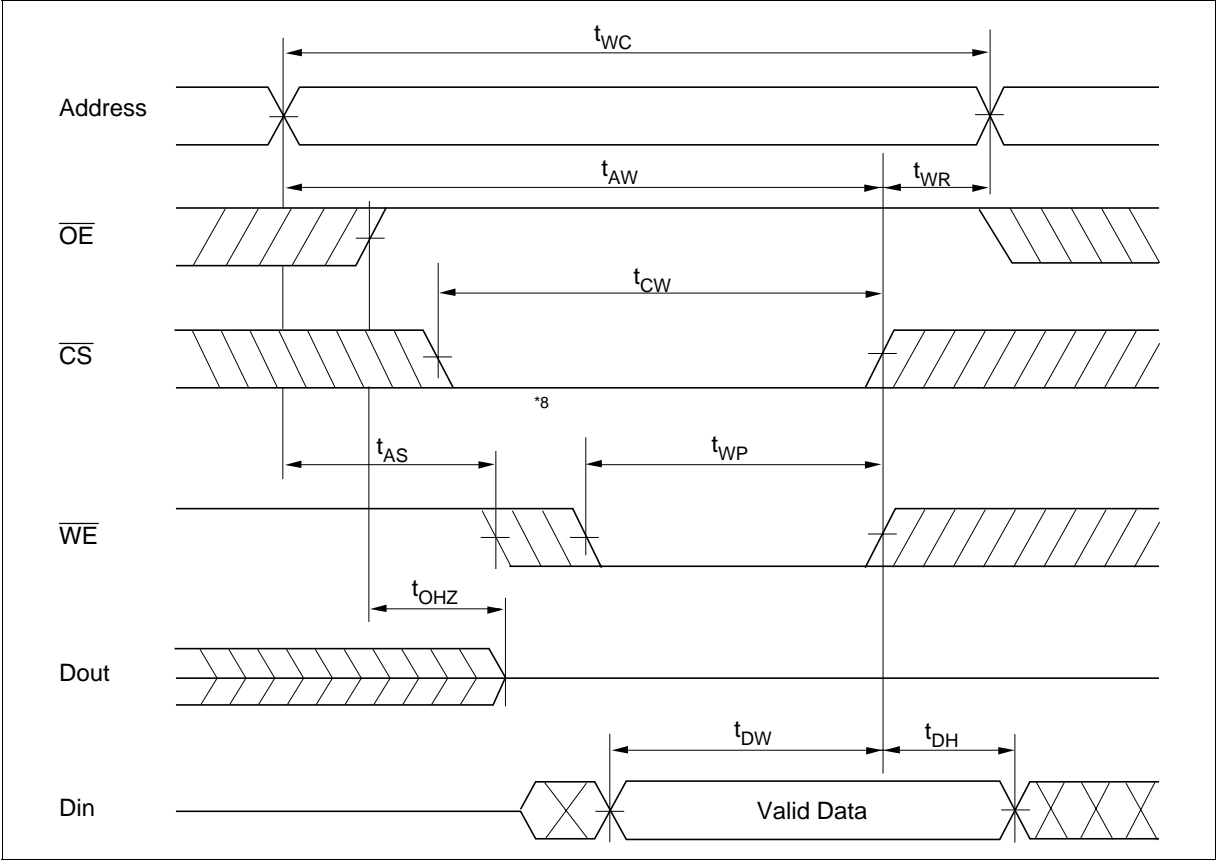
12. In the write cycle with \overline{OE} low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention. $t_{WP} \geq t_{DW} \text{ min} + t_{WHZ} \text{ max}$

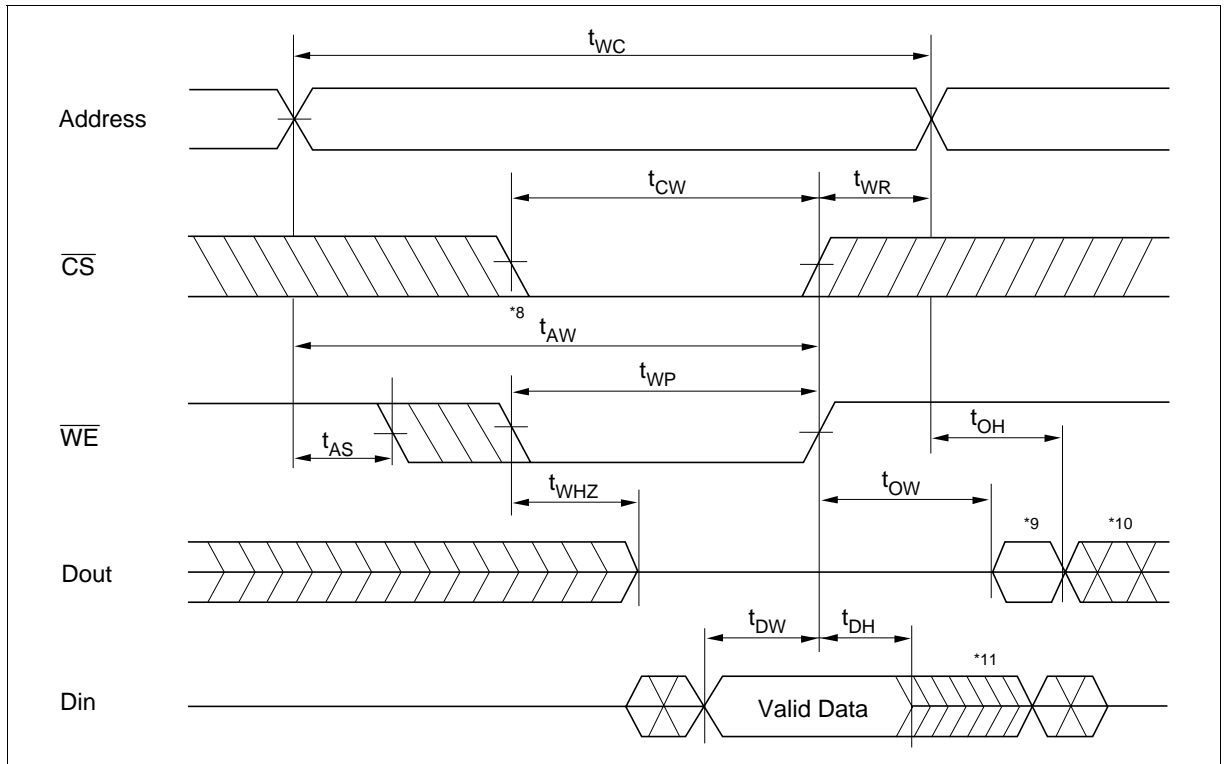
Timing Waveforms

Read Timing Waveform ($\overline{WE} = V_{IH}$)



Write Timing Waveform (1) ($\overline{\text{OE}}$ Clock)



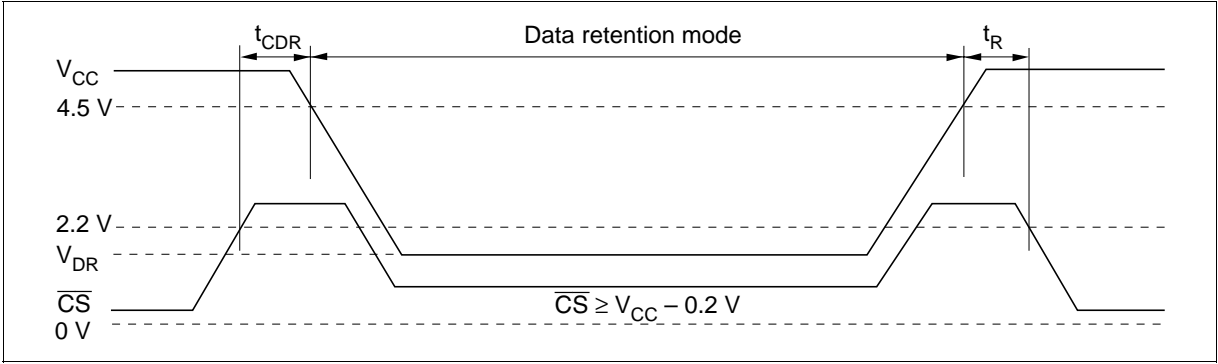
Write Timing Waveform (2) ($\overline{\text{OE}}$ Low Fixed)

Low V_{CC} Data Retention Characteristics (Ta = -20 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions*3
V _{CC} for data retention	V _{DR}	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2 \text{ V}$, Vin ≥ 0 V
Data retention current	I _{CCDR}	—	1*4	50*1	μA	V _{CC} = 3.0 V, Vin ≥ 0 V $\overline{CS} \geq V_{CC} - 0.2 \text{ V}$
		—	1*4	15*2	μA	
Chip deselect to data retention time	t _{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t _R	t _{RC} *5	—	—	ns	

- Notes:
- 1. For L-version and 20 μA (max.) at Ta = -20 to +40°C.
 - 2. For L-SL-version and 3 μA (max.) at Ta = -20 to +40°C.
 - 3. \overline{CS} controls address buffer, \overline{WE} buffer, \overline{OE} buffer, and Din buffer. In data retention mode, Vin levels (address, \overline{WE} , \overline{OE} , I/O) can be in the high impedance state.
 - 4. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and specified loading, and not guaranteed.
 - 5. t_{RC} = read cycle time.

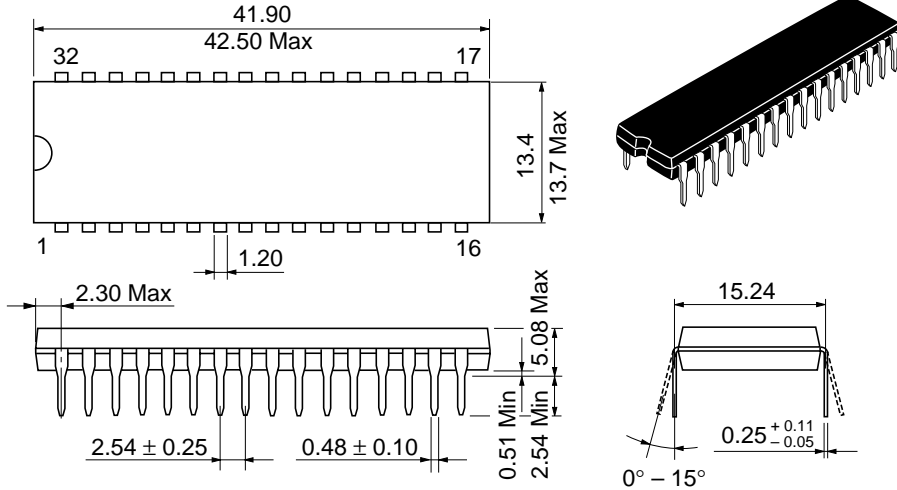
Low V_{CC} Data Retention Timing Waveform (\overline{CS} Controlled)



Package Dimensions

HM628512CLP Series (DP-32)

Unit: mm

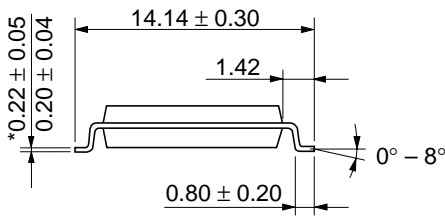
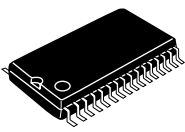
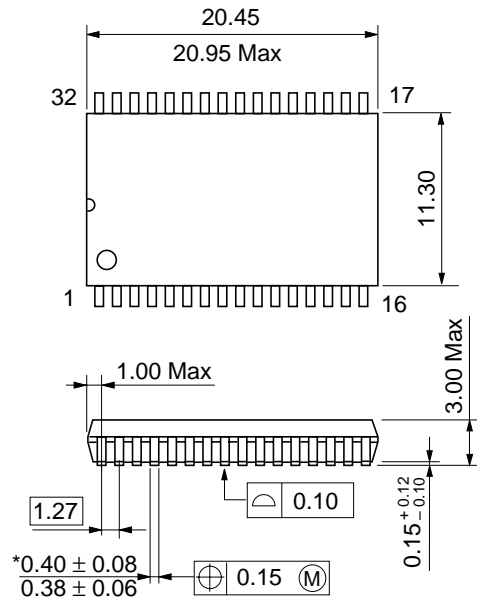


Hitachi Code	DP-32
JEDEC	—
EIAJ	Conforms
Mass (reference value)	5.1 g

Package Dimensions (cont.)

HM628512CLFP Series (FP-32D)

Unit: mm



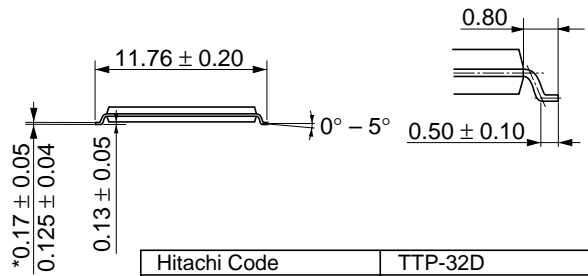
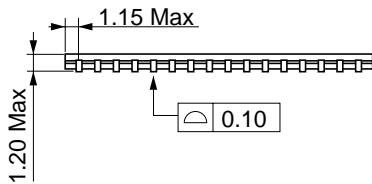
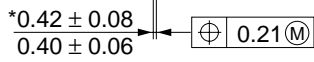
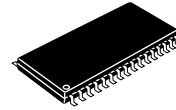
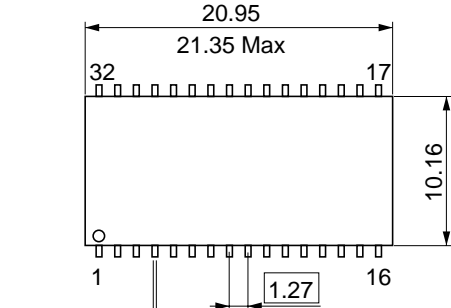
*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-32D
JEDEC	Conforms
EIAJ	—
Mass (reference value)	1.3 g

Package Dimensions (cont.)

HM628512CLTT Series (TTP-32D)

Unit: mm



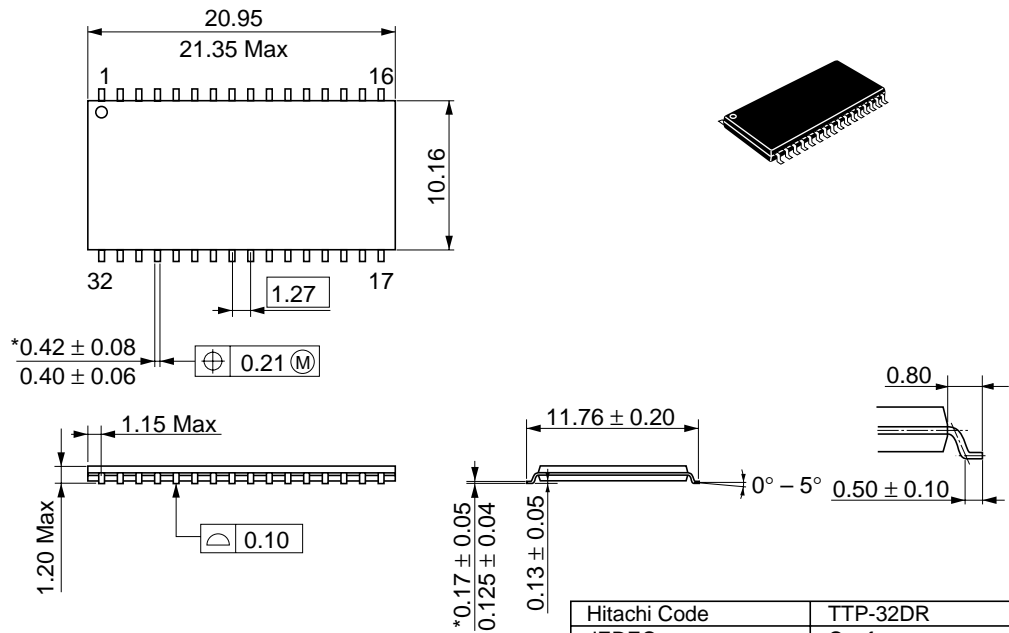
*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-32D
JEDEC	Conforms
EIAJ	—
Mass (reference value)	0.51 g

Package Dimensions (cont.)

HM628512CLRR Series (TTP-32DR)

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-32DR
JEDEC	Conforms
EIAJ	—
Mass (reference value)	0.51 g

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