DEVICE
PERFORMANCE
SPECIFICATION

KODAK KAF-16802CE
KODAK KAF-16802LE
Image Sensor

4080 (H) x 4080 (V)
Full-Frame CCD Image Sensor
With Square Pixels

January 22, 2003
Revision 1

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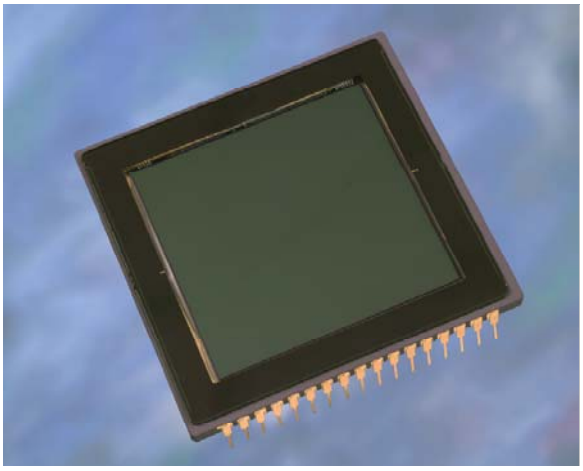
SUMMARY SPECIFICATION

KODAK KAF-16802CE/LE Image Sensor 4080 (H) x 4080 (V) Full-Frame CCD Color Image Sensor



Description

The KAF-16802CE/LE is a high performance array CCD (charge coupled device) image sensor with 4080(H) x 4080(V) photoactive pixels designed for a wide range of color and monochrome image sensing applications including digital imaging. Each pixel contains anti-blooming protection by means of a lateral overflow drain thereby preventing image corruption during high light level conditions. In the color version each of the 9µm square pixels are selectively covered with red, green or blue pigmented filters for color separation. The photoactive pixels are surrounded by a border of buffer and light shielded pixels as shown in Figure 1. Total chip size is 38.60 mm x 37.76 mm and is housed in a 34 pin, 2.010" wide DIL ceramic package with 0.100" pin spacing.

Parameter	Typical Value
Architecture	Full Frame CCD; with Square Pixels
Total Number of Pixels	4145 (H) x 4128 (V) = 17.1M
Number of Effective Pixels	4098 (H) x 4098 (V) = 16.8M
Number of Active Pixels	4080 (H) x 4080 (V) = 16.6M
Pixel Size	9µm (H) x 9µm (V)
Imager Size	51.9mm (diagonal)
Chip Size	38.60mm (H) x 37.76mm (V)
Aspect Ratio	1:1
Saturation Signal	94 K e^-
Charge to Voltage Conversion	17.5µV/e^-
Quantum Efficiency	
red, green, blue	0.23, 0.19, 0.17
Total Noise	21 e^-
Dark Signal	2.7 mV
Dark Current Doubling Temperature	6.3 dC
Linear Dynamic Range	73 dB
Charge Transfer Efficiency	0.999999
Blooming Protection @4ms integration time	1600 x saturation exposure
Maximum Data Rate	20 MHz

All parameters above are specified at T = 20°C

REVISION NO.: 1
EFFECTIVE DATE: January 22, 2003

DEVICE DESCRIPTION

Architecture

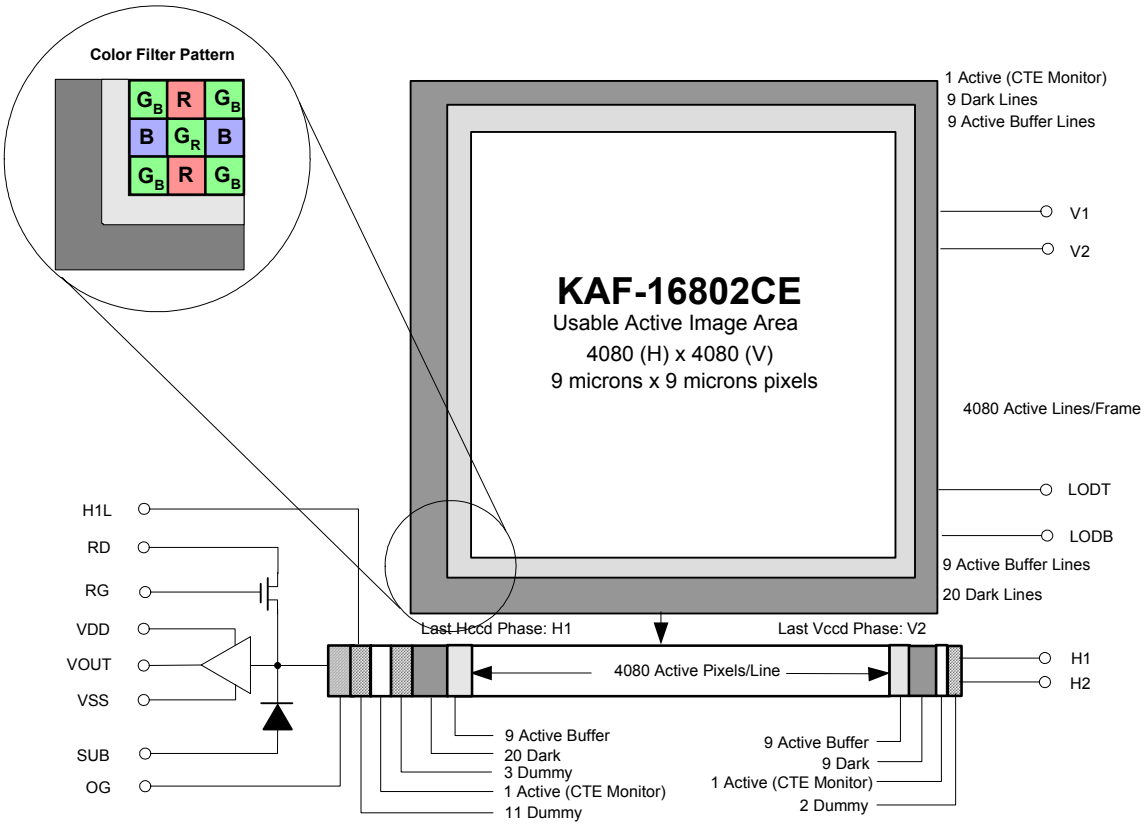


Figure 1 - Sensor Architecture

Dark Reference Pixels

Surrounding the periphery of the device is a border of light shielded pixels. This includes 20 leading and 9 trailing pixels on every line excluding dummy pixels. There are also 20 full dark lines at the start of every frame and 9 full dark lines at the end of each frame. Under normal circumstances, these pixels do not respond to light. However, dark reference pixels in close proximity to an active pixel, or the outer bounds of the chip (including the first two lines out), can scavenge signal depending on light intensity and wavelength.

Active Buffer Pixels

The first 9 pixels in from any dark reference regions are classified as active buffer pixels. These pixels are light sensitive but tend to have inconsistent spectral responsivities than the remainder of the array. Active buffer pixels are not tested for defects and uniformity.

Dummy Pixels

Within the horizontal shift register are 11 leading and 2 trailing additional shift phases, which are not associated with a column of pixels within the vertical register. These pixels contain only horizontal shift register dark current

signal and do not respond to light. A few leading dummy pixels may scavenge false signal depending on operating conditions.

CTE Monitor Pixels

Two CTE test columns, one on each of the leading and trailing ends and one CTE test row are included for manufacturing test purposes.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the device. These photon induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons are discharged into the lateral overflow drain to prevent crosstalk or 'blooming'. During the integration period, the V1 and V2 register clocks are held at a constant (low) level

Charge Transport

The integrated charge from each photogate is transported to the output using a two step process. Each line (row) of charge is first transported from the vertical CCD's to a horizontal CCD register using the V1 and V2 register clocks. The horizontal CCD is presented a new line on the falling edge of V2 while H1 is held high. The horizontal CCD's then transport each line, pixel by pixel, to the output structure by alternately clocking the H1 and H2 pins in a complementary fashion. A separate connection to the last H1 phase (H1L) is provided to improve the transfer speed of charge to the floating diffusion. On each falling edge of H1 a new charge packet is dumped onto a floating diffusion and sensed by the output amplifier.

Horizontal Register

Output Structure

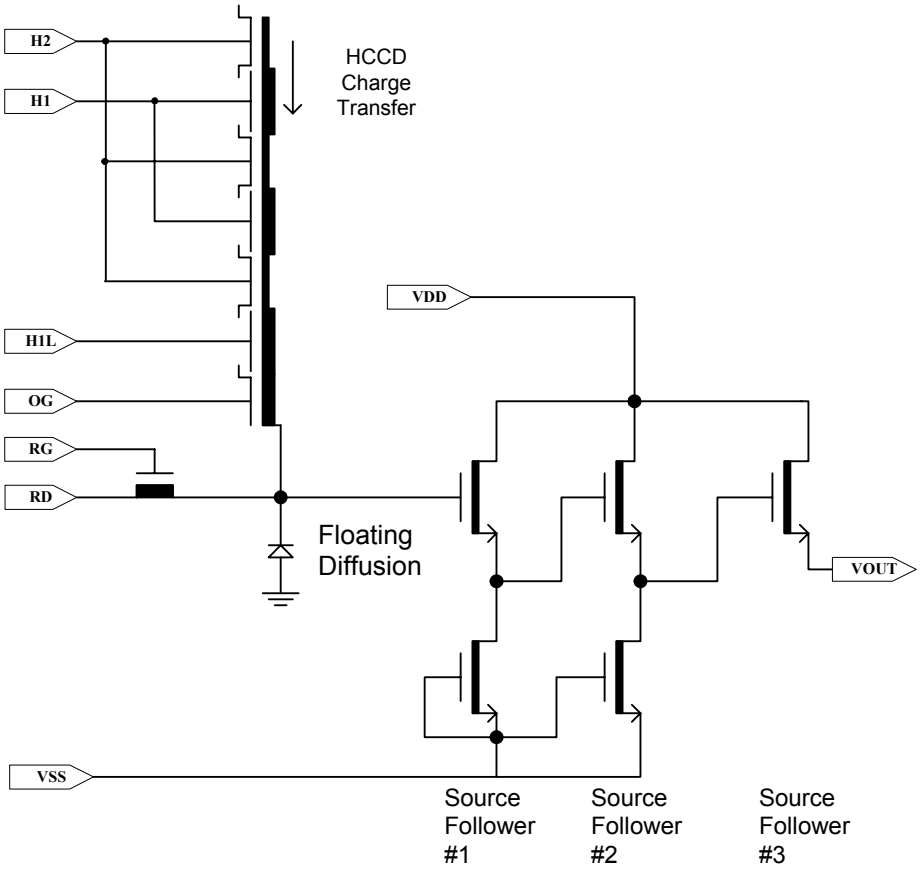


Figure 2 - Output Architecture

Charge presented to the floating diffusion (FD) is converted into a voltage and is current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the FD. Once the signal has been sampled by the system electronics, the reset gate (RG) is clocked to remove the signal and FD is reset to the potential applied by reset drain (RD). Increased signal at the floating diffusion reduces the voltage seen at the output pin. To activate the output structure, an off-chip load must be added to the VOUT pin of the device. See Figure 3.

Output Load

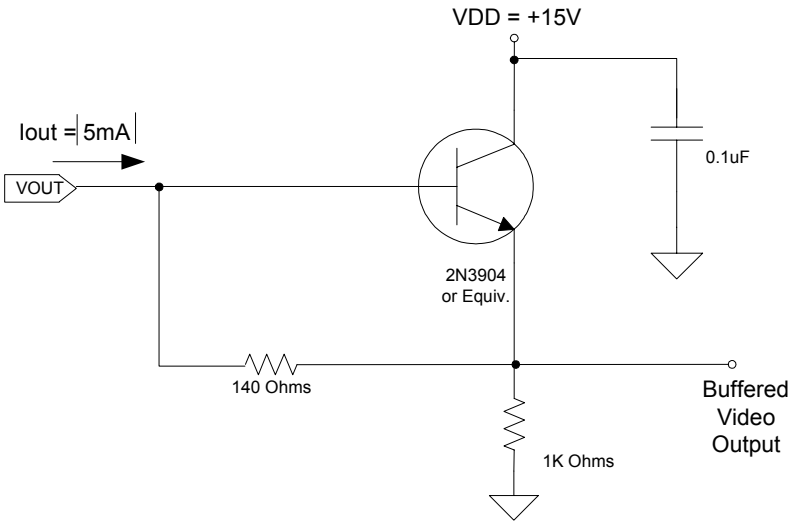
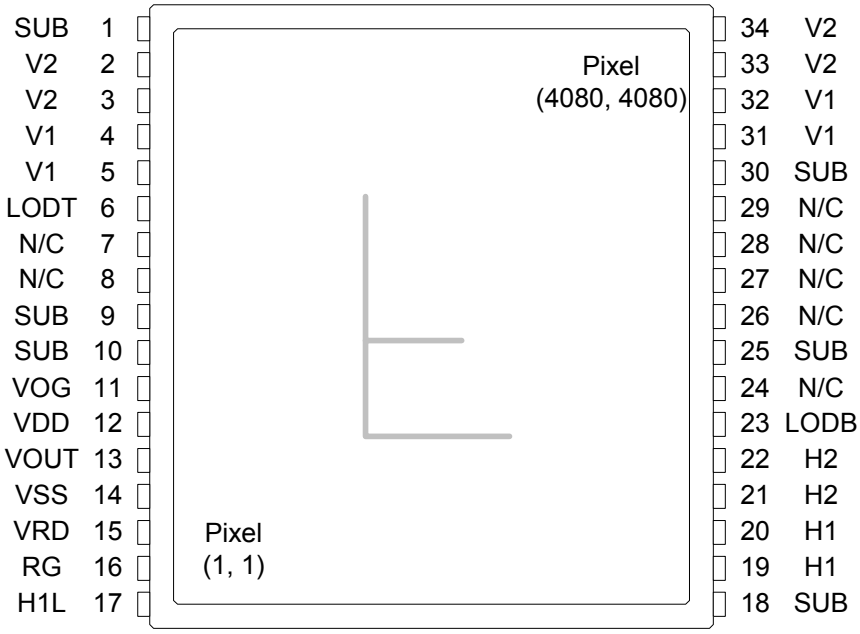


Figure 3 – Recommended Output Structure Load Diagram

Component values may be revised based on operating conditions and other design considerations.

Physical Description

Pin Description and Device Orientation



Pin	Name	Description	Pin	Name	Description
1	SUB	Substrate	34	V2	Vertical Phase 2
2	V2	Vertical Phase 2	33	V2	Vertical Phase 2
3	V2	Vertical Phase 2	32	V1	Vertical Phase 1
4	V1	Vertical Phase 1	31	V1	Vertical Phase 1
5	V1	Vertical Phase 1	30	SUB	Substrate
6	LODT	Lateral Overflow Drain Top	29	N/C	No Connection
7	N/C	No Connection	28	N/C	No Connection
8	N/C	No Connection	27	N/C	No Connection
9	SUB	Substrate	26	N/C	No Connection
10	SUB	Substrate	25	SUB	Substrate
11	OG	Output Gate	24	N/C	No Connection
12	VDD	Output Amplifier Supply	23	LODB	Lateral Overflow Drain Bottom
13	VOUT	Video Output	22	H2	Horizontal Phase 2
14	VSS	Output Amplifier Return	21	H2	Horizontal Phase 2
15	RD	Reset Drain	20	H1	Horizontal Phase 1
16	RG	Reset Gate	19	H1	Horizontal Phase 1
17	H1L	Horizontal Phase 1, Last Gate	18	SUB	Substrate

The pins are on a 0.100” spacing

PERFORMANCE

Image Performance Operational Conditions

Description	Condition - Unless otherwise noted	Notes
Frame time ($t_{readout}$)	1928 msec	Includes overclock pixels
Integration time (t_{int})	250 msec	
Horizontal clock frequency	10 MHz	
Temperature	20°C	Room temperature
Mode	integrate – readout cycle	
Operation	Nominal operating voltages and timing With vertical pulse width t_{VW} = 15µs	

Imaging Performance Specifications

Description	Symbol	Min.	Typ.	Max.	Units	Notes	Sample Plan
Saturation Signal	Vsat Ne^-_{sat} Q/V	1400 80K	1650 94K 17.5		mV e^- uV/e^-	1	die
Quantum Efficiency red green blue	Rr Rg Rb		23 19 17		%QE	3	die
High Level Photoresponse Non-Linearity	PRNL			2	%	2	die
Photo Response Non-Uniformity	PRNU red PRNU g, b		10 10	30 20	%p-p	3	die
Dark Signal	Vdark		2.7	5.9	mV	4	die
Dark Signal Non-Uniformity	DSNU		1.5	10	mV p-p	5	die
Dark Signal Doubling Temperature	ΔT	5	6.3	7	°C		design
Total Noise	N		21	60	e^- rms	6	design
Linear Dynamic Range	DR		73		dB	7	design
Red-Green Hue Shift	RGHueUnif		5	15	%	8	die
Blue-Green Hue Shift	BGHueUnif		5	15	%	8	die

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Sample Plan
Horizontal Charge Transfer Efficiency	HCTE	0.999995	0.999999			9	die
Blooming Protection	X_ab		1600		x Esat	10	design
DC Offset, output amplifier	Vodc	7.5	8	8.5	V	11	die
Output Amplifier Bandwidth	f_{-3dB}	100	122	160	Mhz	12	die
Output Impedance, Amplifier	R_{OUT}	100	130	160	Ohms		die
Hclk Feedthru	V_{hft}	-30	5	30	mV	13	die
Reset Feedthru	V_{rft}		750		mV	14	design

Notes:

1. Increasing output load currents to improve bandwidth will decrease these values.
2. Worst case deviation between Vsat/2 and Vsat relative to a linear fit applied between Vsat/2 ± Vsat/8 signal levels (center ¼ of data).
3. Difference between the maximum and minimum average signal levels of 111 x 111 blocks within the sensor on a per color basis as a % of average signal level.
4. T=40°C. Average non-illuminated signal with respect to over-clocked horizontal register signal.
5. T=40°C. Absolute difference between the maximum and minimum average signal levels of 111 x 111 blocks within the sensor.
6. rms deviation of a multi-sampled pixel measured in the dark including amplifier and system noise sources.
7. 20log(Vsat/V_N) - see Note 6 and note 1. V_N = N * nominal charge to voltage
8. Gradual variations in hue (red with respect to green pixels and blue with respect to green pixels) in regions of interest (111 x 111 blocks) within the sensor. Does not apply to the monochrome sensor.
9. Measured per transfer at Vsat min. Typically, no degradation in CTE is observed up to 10 MHz.
10. X_ab is the number of times above the Vsat illumination level that the sensor will bloom by spot size doubling. The spot size is 10% of the imager height. X_ab is measured at 4msec.
11. Video level offset with respect to ground
12. Last stage only. Assumes 10pF off-chip load.
13. Amount of artificial signal due to H1 coupling.
14. Amplitude of feedthrough pulse in VOUT due to RG coupling.

Typical Performance Curves

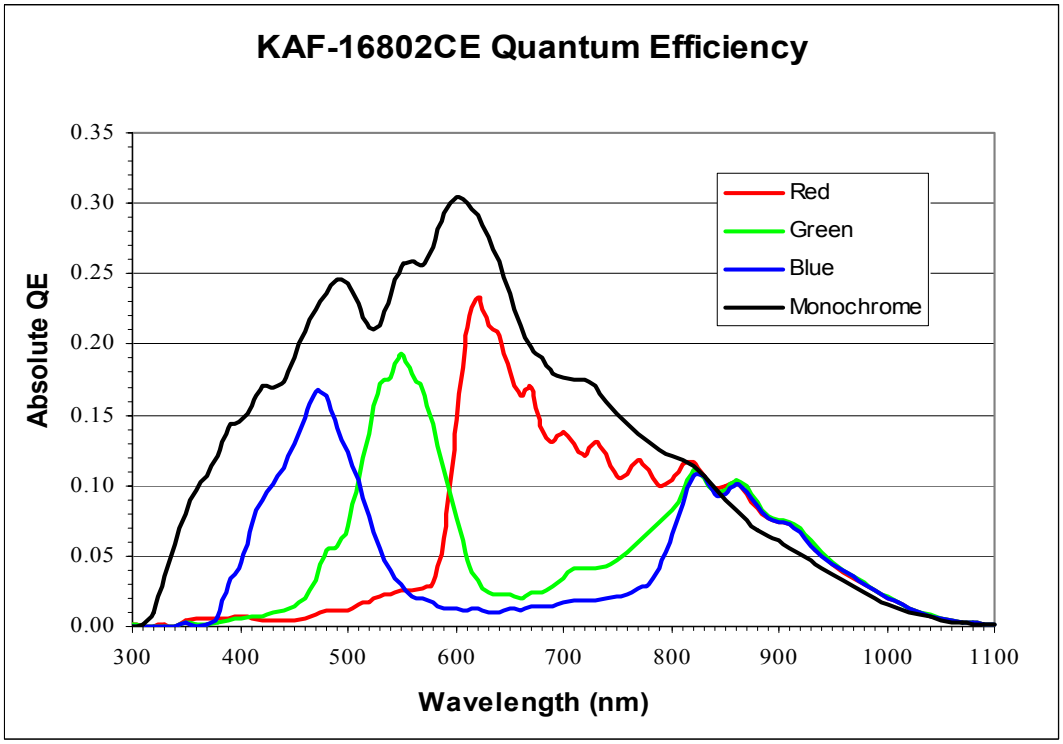


Figure 4 – Typical Quantum Efficiency

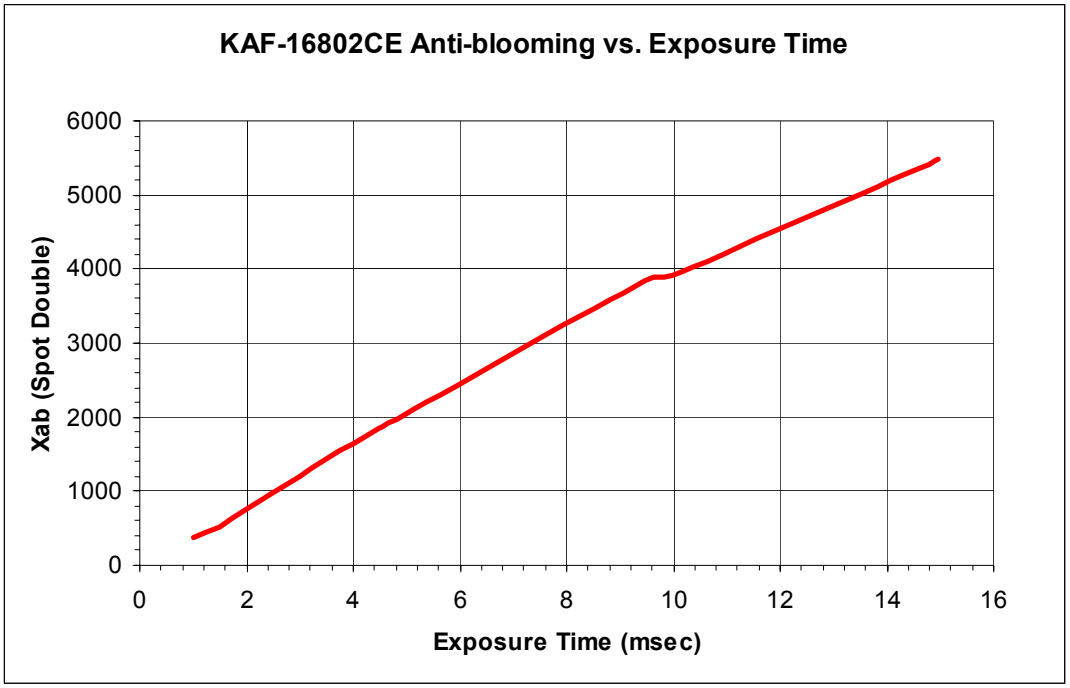


Figure 5 – Typical Blooming Performance

Defect Definitions

Defect Operational Conditions

All defect tests performed at T=25°C, t_{int} = 250 msec and $t_{readout}$ = 1928 msec

Defect Specifications

Classification	Points	Clusters	Single Columns	Includes dead columns
Standard Quality (SQ)	≤3,000	≤40	≤15	yes

Point Defects

A pixel which deviates by more than 7mV above or below neighboring pixels under non-illuminated conditions

-- OR --

A pixel which deviates by more than 7% above or 11% below neighboring pixels under illuminated conditions

Cluster Defect

A grouping of not more than 10 adjacent point defects

Cluster defects are separated by no less than 4 good pixels in any direction

Column Defect

A grouping of 6 or more point defects along a single column

-- OR --

A column which deviates by more than 0.7mV above or below neighboring columns under non-illuminated conditions

-- OR --

A column which deviates by more than 1.5% above or below neighboring columns under illuminated conditions

Column defects are separated by no less than 4 good columns. No multiple column defects (double or more) will be permitted.

Column and cluster defects are separated by at least 4 good columns in the x direction.

Dead Columns

A column which deviates by more than 50% below neighboring columns under illuminated conditions

Saturated Columns

A column which deviates by more than 100mV above neighboring columns under non-illuminated conditions. No saturated columns are allowed.

OPERATION

Absolute Maximum Ratings

Description	Symbol	Minimum	Maximum	Units	Notes
Diode Pin Voltages	Vdiode	0	18	V	1,2
Gate Pin Voltages - Type 1	Vgate1	-14	14	V	1,3
Gate Pin Voltages - Type 2	Vgate2	0	18	V	1,4
Inter-Gate Voltages	V_{g-g}		14	V	5
V1, H2 Voltages	V_{V-H}		14	V	6
V1, V2 – LOD Voltages	V_{V-L}		20	V	7
Output Bias Current	Iout		-10	mA	8
Output Load Capacitance	Cload		15	pF	8
Operating Temperature	T_{OP}	0	70	°C	9
Humidity	RH	5	90	%	10
LOD Diode Voltage	V_{LOD}	0	11	V	11

Notes:
1. Referenced to pin SUB
2. Includes pins: RD, VDD, VSS, VOUT.
3. Includes pins: V1, V2, H1, H1L, H2.
4. Includes pins with ESD protection: RG, OG.
5. Voltage difference between overlapping gates. Includes: V1 to V2; H1, H1L to H2; H1L to OG; V1 to H2.
6. Voltage difference between non-overlapping gates. Includes: V1 to H1, H1L; V2, OG to H2.
7. Voltage difference between V1, V2 gates and LODT, LODB diode.
8. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher currents and lower load capacitance at the expense of reduced gain (sensitivity). Operation at these values will reduce MTTF.
9. Noise performance will degrade at higher temperatures.
10. T=20°C. Excessive humidity will degrade MTTF.
11. V1 and V2 are biased to –9.2V.

Power-up Sequence

The sequence chosen to perform an initial power-up is not critical for device reliability. A coordinated sequence may minimize noise and the following sequence is recommended:

1. Connect the ground pins (SUB).
2. Supply the appropriate biases and clocks to the remaining pins.

DC Bias Operating Conditions

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Reset Drain	RD	11.3	11.5	11.7	V	I_{RD} = 0.01	
Output Amplifier Return	VSS	0.5	1.0	1.5	V	I_{SS} = 3.0	
Output Amplifier Supply	VDD	14.5	15.0	15.5	V	I_{OUT} + I_{SS}	
Substrate	SUB		0		V	0.01	
Output Gate	OG	0.8	1.0	1.2	V	0.01	
Lateral Drain	LODT,LODB	9.5	10.0	10.5	V	0.01	
Video Output Current	I_{OUT}		-5	-10	mA		1

Notes:
1. An output load sink must be applied to VOUT to activate output amplifier - see Figure 3.

AC Operating Conditions

Clock Levels

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Effective Capacitance	Notes
V1 Low Level	V1L	Low	-9.2	-9.0	-8.8	V	595 nF	1
V1 High Level	V1H	High	1.8	2.0	2.2	V		1
V2 Low Level	V2L	Low	-9.2	-9.0	-8.8	V	587nF	1
V2 High Level	V2H	High	1.8	2.0	2.2	V		1
H1 Low Level	H1L	Low	-4.7	-4.5	-4.3	V	430 pF	1
H1 High Level	H1H	High	3.3	3.5	3.7	V		1
H1L Low Level	$H1L_{low,}$	Low	-6.7	-6.5	-6.3	V	10 pF	1
H1L High Level	$H1L_{high}$	High	3.3	3.5	3.7	V		1
H2 Low Level	H2L	Low	-5.2	-5.0	-4.8	V	370 pF	1
H2 High Level	H2H	High	2.8	3.0	3.2	V		1
RG Low Level	RGL	Low	3.3	3.5	3.7	V	6 pF	1
RG High Level	RGH	High	9.8	10	10.2	V		1

Notes:
1. All pins draw less than 10µA DC current. Capacitance values relative to SUB (substrate).

Timing Requirements

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
H1, H2 Clock Frequency	f_H		10	20	MHz	1, 2
V1, V2 Clock Frequency	f_V		25	50	kHz	1, 2
H1L, H1, H2 Rise, Fall Times	t_{Hr} , t_{Hf}	5		10	%	3, 8
V1, V2 Rise, Fall Times	t_{Vr} , t_{Vf}	5		10	%	3
V1 - V2 Cross-over	V_{VCR}	-1	0		V	
H1 - H2 Cross-over	V_{HCR}	30	50	70	%	4
Pixel Period (1 Count)	t_e	50	100		ns	2
H1, H2 Setup Time	t_{HS}	1	5		µs	
RG Clock Pulse Width	t_{RGw}	10	20		ns	5
RG Rise, Fall Times	t_{RGr} , t_{RGf}	5		10	%	3
V1, V2 Clock Pulse Width	t_{Vw}	15	18		µs	2, 7
H1L – VOUT Delay	t_{HV}		5		ns	
RG - VOUT Delay	t_{RV}		5		ns	
Readout Time	$t_{readout}$	983.5	1897		ms	7, 9
Integration Time	t_{int}					6, 7
Line Time	t_{line}	238.3	459.6		µs	7
Flush Time	t_{flush}	124	149		ms	

Notes:

1. 50% duty cycle values.
2. CTE will degrade above the nominal frequency.
3. Relative to the pulse width (based on 50% of high/low levels).
4. Relative to clock amplitude.
5. RG should be clocked continuously.
6. Integration time is user specified.
7. Longer times will degrade noise performance.
8. The maximum specification or 10nsec whichever is greater based on the frequency of the horizontal clocks.
9. $t_{readout} = t_{line} * 4128$ lines.

TIMING DIAGRAMS

Frame Timing

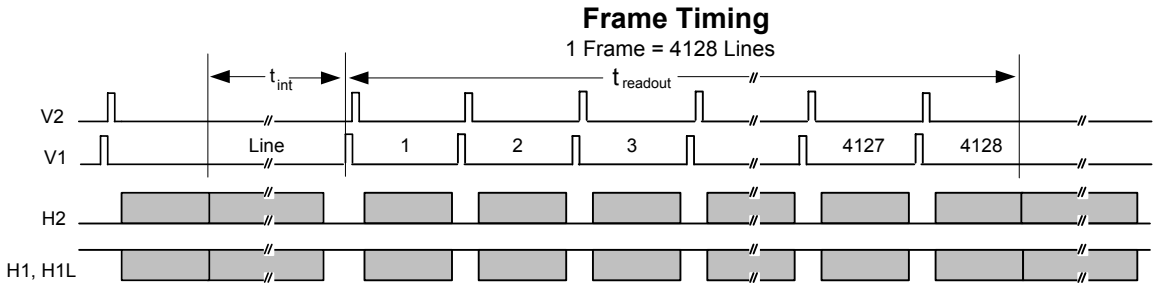


Figure 6 - Frame Timing

Line Timing

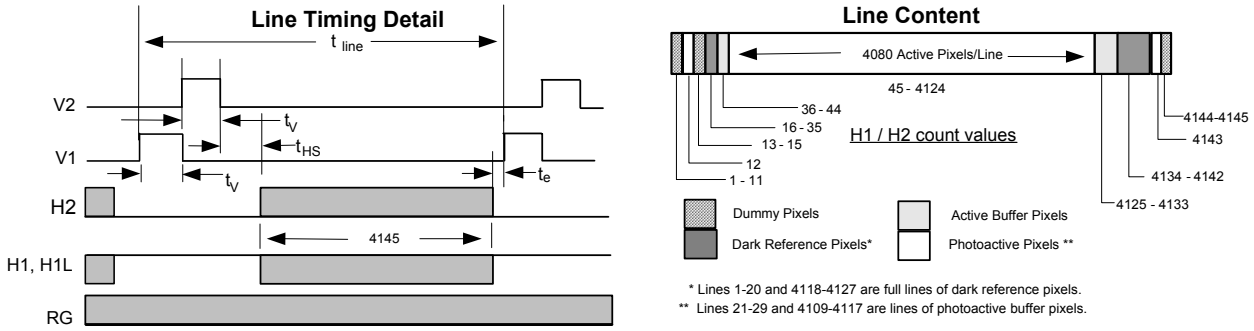


Figure 7 - Line Timing

Pixel Timing

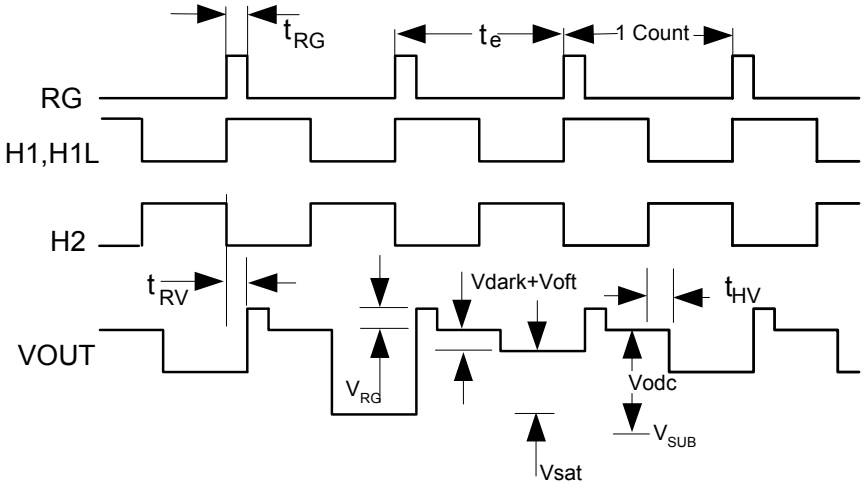


Figure 8 – Pixel Timing

MODE OF OPERATION

Power-up Flush Cycle

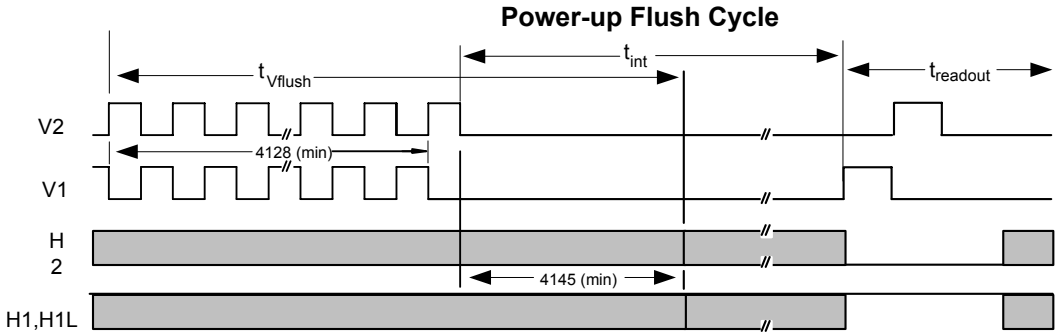


Figure 9 – Power-up Flush Cycle

STORAGE AND HANDLING

Storage Conditions

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	-20	70	°C	1

1. Long-term storage toward the maximum temperature will accelerate color filter degradation.

ESD

Caution: This device contains limited protection against Electrostatic Discharge (ESD). Devices should be handled in accordance with strict ESD procedures for class 0 devices (JESD22 Human Body Model, or Class A (JESD22 Machine Model). See Application Note MTD/PS-0224.

Cover glass Care

Caution: Improper cleaning of the cover glass may damage these devices. Refer to Application Note MTD/PS-0237 “Cover Glass Cleaning Procedure for Image Sensors”

Soldering Recommendations

Partial Heating Method: 280 degrees Centigrade maximum pin temperature; 10 seconds maximum duration per pin.

MECHANICAL DRAWINGS

Package

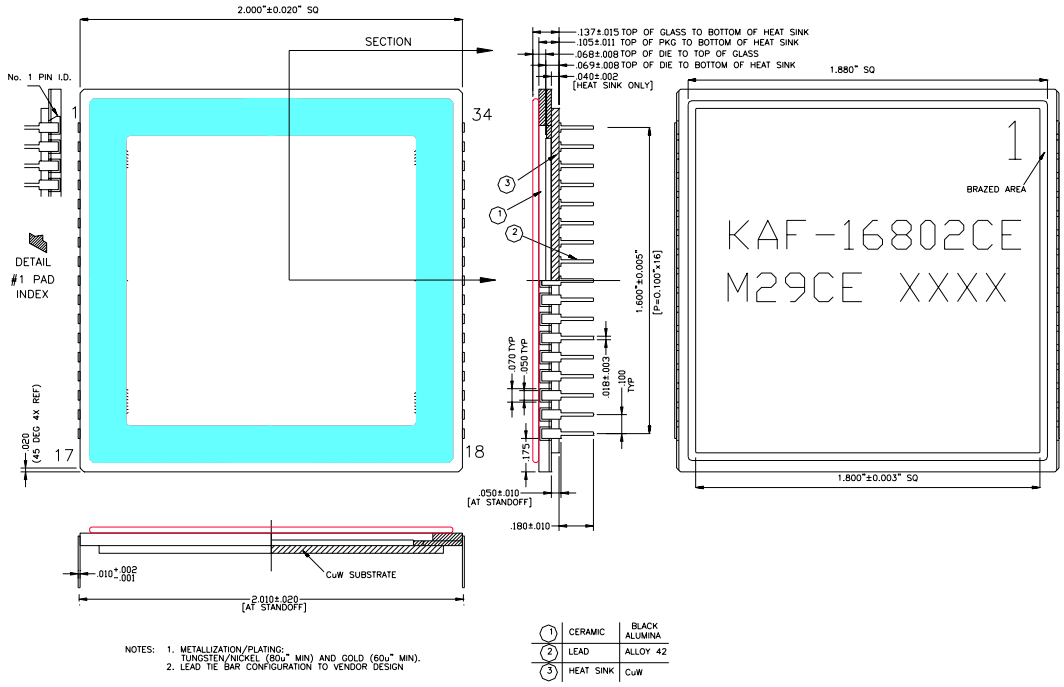


Figure 10 – Package Drawing

Glass

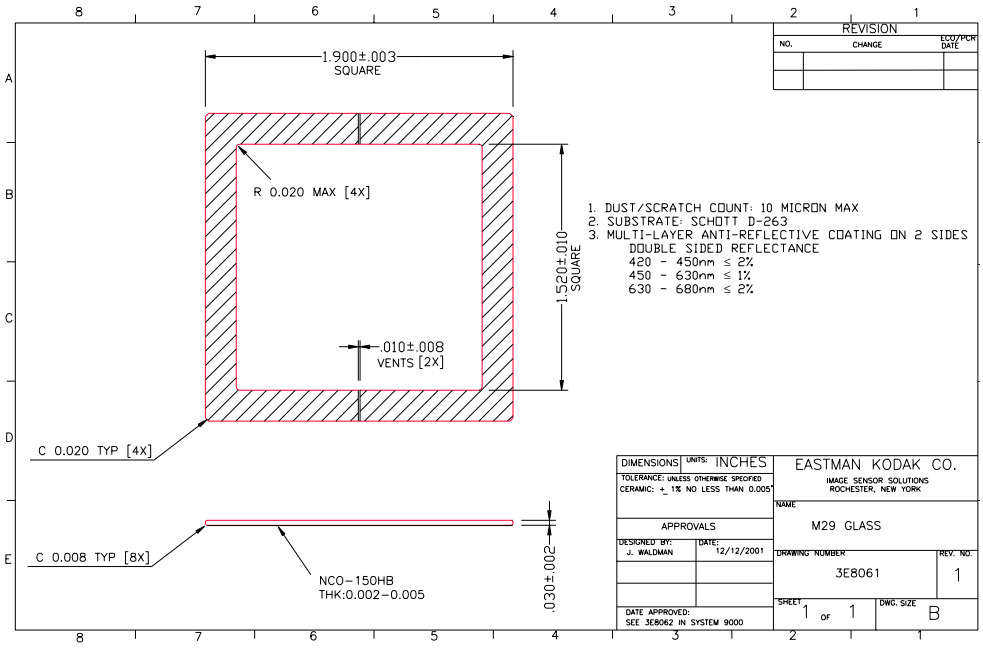


Figure 11 – Glass Drawing

QUALITY ASSURANCE AND RELIABILITY

Quality Strategy: All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

Replacement: All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.

Liability of the Supplier: A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer.

Liability of the Customer: Damage from mechanical (scratches or breakage), electrostatic discharge (ESD) damage, or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Cleanliness: Devices are shipped free of mobile contamination inside the package cavity. Immovable particles and scratches that are within the imager pixel area and the corresponding cover glass region directly above the pixel sites are also not allowed. The cover glass is highly susceptible to particles and other contamination. Touching the cover glass must be avoided. See ISS Application Note MTD/PS-0237, Cover Glass Cleaning, for further information.

ESD Precautions: Devices are shipped in static-safe containers and should only be handled at static-safe workstations. See ISS Application Note MTD/PS-0224 for handling recommendations.

Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

Test Data Retention: Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical: The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

ORDERING INFORMATION

Available Part Configurations

Type	Description	Glass Configuration
KAF-16802CE	Color	Double Anti-Reflective, sealed
KAF-16802LE	Monochrome	Double Anti-Reflective, sealed

Please contact Image Sensor Solutions for available part numbers.

Address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010
Phone: (585) 722-4385
Fax: (585) 477-4947
E-mail: imagers@kodak.com

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

REVISION CHANGES

Revision Number	Release Date	Description of Changes
1	01/17/03	Initial Release.