TC835

Personal Computer Data Acquisition A/D Converter

Features

- Upgrade of Pin-Compatible TC7135, ICL7135
- 200kHz Operation
- Single 5V Operation With TC7660
- Multiplexed BCD Data Output
- UART and Microprocessor Interface
- Control Outputs for Auto-Ranging
- Input Sensitivity: 100µV
- No Sample and Hold Required

Applications

- Personal Computer Data Acquisition
- Scales, Panel Meters, Process Controls
- HP-IL Bus Instrumentation

Device Selection Table

Part Number	Package	Temperature Range
TC835CBU	64-Pin PQFP	0°C to +70°C
TC835CKW	44-Pin PQFP	0°C to +70°C
TC835CPI	28-Pin PDIP	0°C to +70°C

Note: Tape and Reel available for 44-Pin PQFP package.

General Description

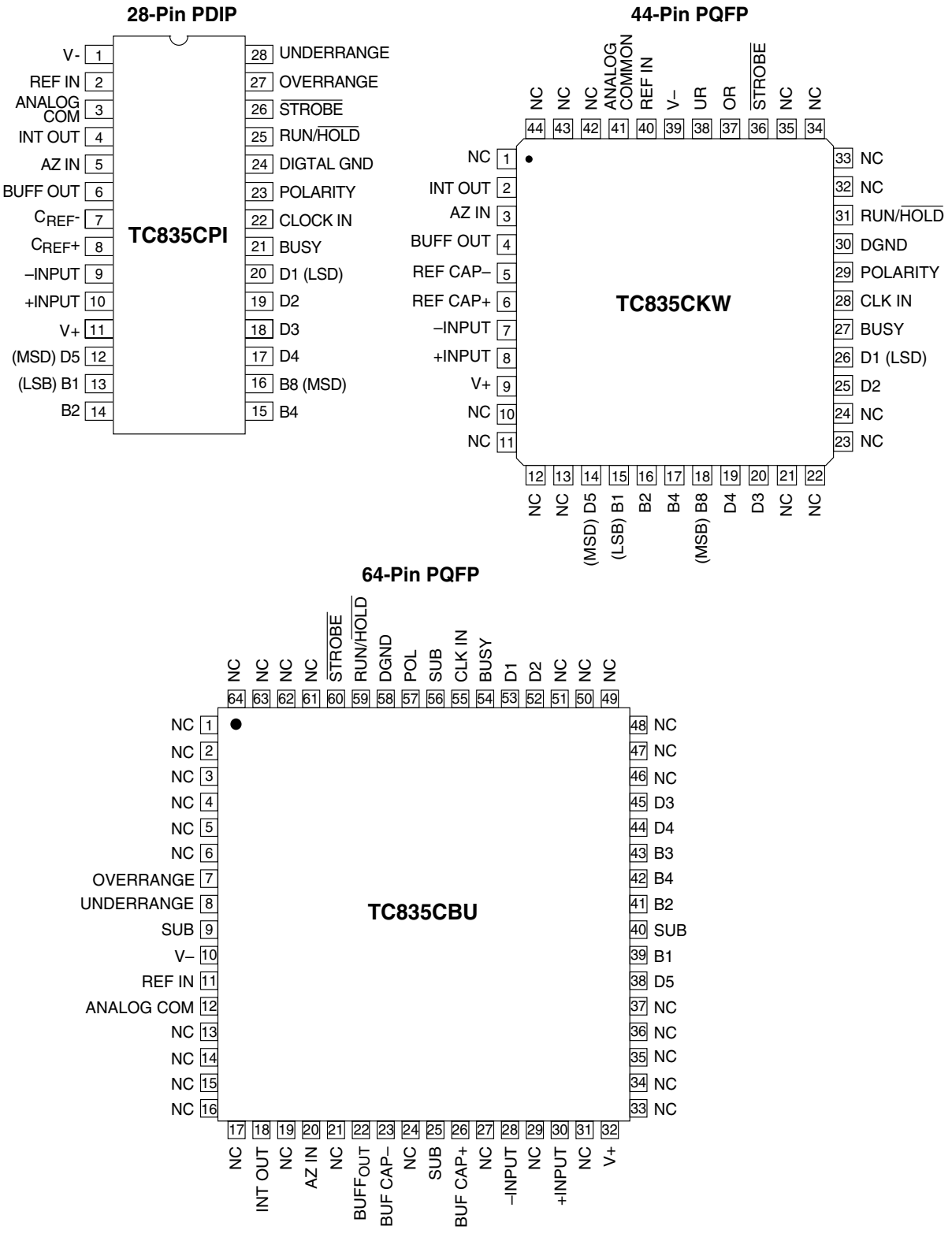
The TC835 is a low power, 4-1/2 digit (0.005% resolution), BCD analog to digital converter (ADC) that has been characterized for 200kHz clock rate operation. The five conversions per second rate is nearly twice as fast as the ICL7135 or TC7135. The TC835, like the TC7135, does not use the external diode resistor rollover error compensation circuits required by the ICL7135.

The multiplexed BCD data output is perfect for interfacing to personal computers. The low cost, greater than 14-bit high-resolution and 100µV sensitivity makes the TC835 exceptionally cost-effective.

Microprocessor-based data acquisition systems are supported by the BUSY and STROBE outputs, along with the RUN/HOLD input of the TC835. The OVERRANGE, UNDERRANGE, BUSY and RUN/HOLD control functions, plus multiplexed BCD data outputs, make the TC835 the ideal converter for µP-based scales, measurement systems and intelligent panel meters.

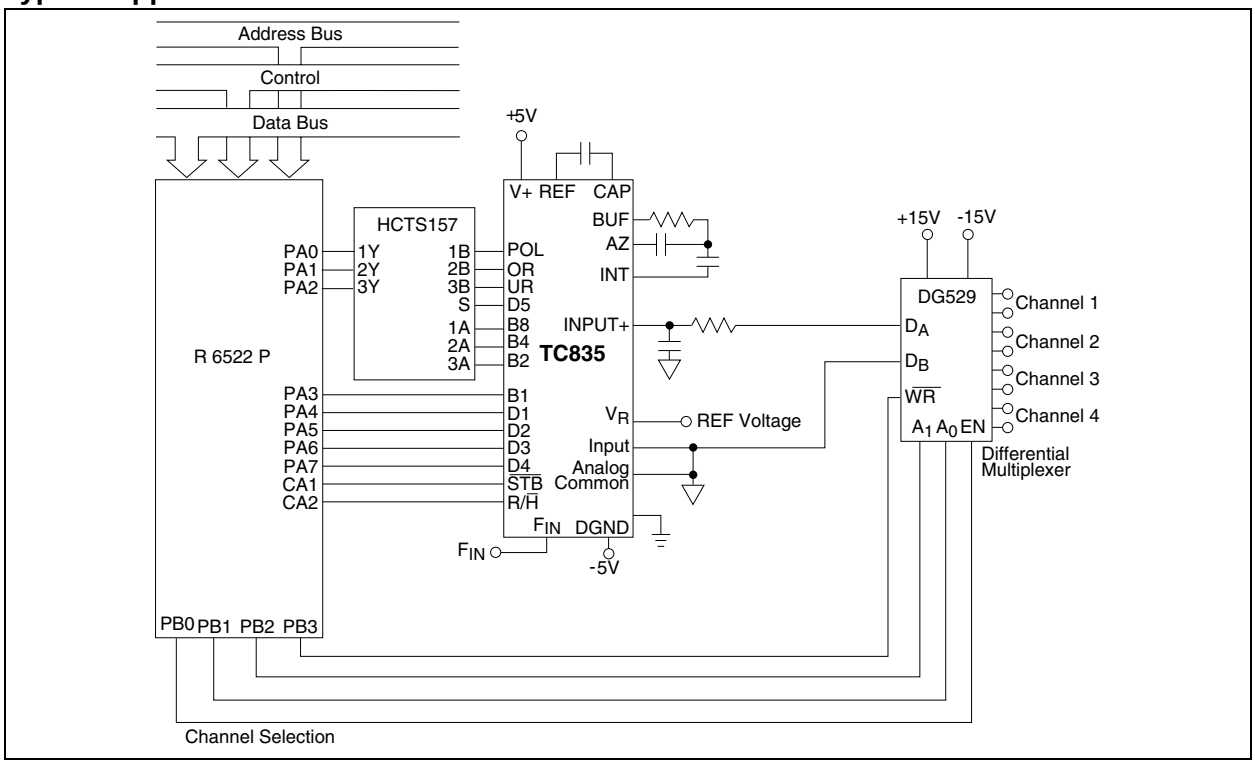
The TC835 interfaces with full function LCD and LED display decoder/drivers. The UNDERRANGE and OVERRANGE outputs may be used to implement an auto-ranging scheme or special display functions.

Package Type



NOTES: 1. NC = No internal connection.
2. Pins 9, 25, 40 and 56 are connected to the die substrate. The potential at these pins is approximately V+. No external connections should be made.

Typical Application



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Positive Supply Voltage ..... +6V
Negative Supply Voltage ..... -9V
Analog Input Voltage (Pin 9 or 10) ... V+ to V– (Note 2)
Reference Input Voltage (Pin 2) ..... V+ to V–
Clock Input Voltage ..... 0V to V^+
Operating Temperature Range.....0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C
Package Power Dissipation ($T_A \leq 70°C$)
28-Pin Plastic DIP 1.14Ω
44-Pin PQFP 1.00Ω
64-Pin PQFP 1.14Ω

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC835 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: T_A = +25°C, F_{CLOCK} = 200kHz, V+ = +5V, V- = -5V, unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Analog						
	Display Reading with Zero Volt Input	-0.0000	±0.0000	+0.0000	Display Reading	**Note 3**, **Note 4**
TC_Z	Zero Reading Temperature Coefficient	—	0.5	2	µV/°C	V_{IN} = 0V, **(Note 5)**
TC_{FS}	Full-Scale Temperature Coefficient	—	—	5	ppm/°C	V_{IN} = 2V; **(Note 5**, **Note 6**
NL	Nonlinearity Error	—	0.5	1	Count	**Note 7**
DNL	Differential Linearity Error	—	0.01	—	LSB	**Note 7**
	Display Reading in Ratiometric Operation	+0.9996	+0.9998	+1.0000	Display Reading	$V_{IN} = V_{REF}$, **(Note 3)**
±FSE	± Full Scale Symmetry Error (Rollover Error)	—	0.5	1	Count	$-V_{IN} = +V_{IN}$, **(Note 8)**
I_{IN}	Input Leakage Current	—	1	10	pA	**Note 4**
e_N	Noise	—	15	—	μV_{P-P}	Peak to Peak Value not Exceeded 95% of Time
Digital						
I_{IL}	Input Low Current	—	10	100	µA	V_{IN} = 0V
I_{IH}	Input High Current	—	0.08	10	µA	V_{IN} = +5V
V_{OL}	Output Low Voltage	—	0.2	0.4	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage;	2.4	4.4	5	V	I_{OH} = 1mA
	B_1, B_2, B_4, B_8, D_1 –D_5 Busy, Polarity, Overrange, Underrange, Strobe	4.9	4.99	5	V	I_{OH} = 10µA
f_{CLK}	Clock Frequency	0	200	1200	kHz	**Note 10**

Note 1: Functional operation is not implied.
2: Limit input current to under 100 µA if input voltages exceed supply voltage.
3: Full scale voltage = 2V.
4: V_{IN} = 0V.
5: $0°C \leq T_A \leq +70°C$.
6: External reference temperature coefficient less than 0.01ppm/°C.
7: $-2V \leq V_{IN} \leq +2V$. Error of reading from best fit straight line.
8: $|V_{IN}| = 1.9959$.
9: Test circuit shown in Figure 1-1.
10: Specification related to clock frequency range over which the TC835 correctly performs its various functions. Increased errors result at higher operating frequencies.

TC835 ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: T_A = +25°C, F_{CLOCK} = 200kHz, V+ = +5V, V- = -5V, unless otherwise specified.						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Power Supply						
V+	Positive Supply Voltage	4	5	6	V	
V–	Negative Supply Voltage	-3	-5	-8	V	
I+	Positive Supply Current	—	1	3	mA	f_{CLK} = 0Hz
I–	Negative Supply Current	—	0.7	3	mA	f_{CLK} = 0Hz
PD	Power Dissipation	—	8.5	30	mΩ	f_{CLK} = 0Hz

Note 1: Functional operation is not implied.
2: Limit input current to under 100 µA if input voltages exceed supply voltage.
3: Full scale voltage = 2V.
4: V_{IN} = 0V.
5: 0°C ≤ T_A ≤ +70°C.
6: External reference temperature coefficient less than 0.01ppm/°C.
7: -2V ≤ V_{IN} ≤ +2V. Error of reading from best fit straight line.
8: $|V_{IN}|$ = 1.9959.
9: Test circuit shown in Figure 1-1.
10: Specification related to clock frequency range over which the TC835 correctly performs its various functions. Increased errors result at higher operating frequencies.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number 28-Pin PDIP	Symbol	Description
1	V-	Negative power supply input.
2	REF IN	External reference input.
3	ANALOG COMMON	Reference point for REF IN.
4	INT OUT	Integrator output. Integrator capacitor connection.
5	AZ IN	Auto zero input. Auto zero capacitor connection.
6	BUFF OUT	Analog input buffer output. Integrator resistor connection.
7	C_{REF}-	Reference capacitor input. Reference capacitor negative connection.
8	C_{REF}+	Reference capacitor input. Reference capacitor positive connection.
9	-INPUT	Analog input. Analog input negative connection.
10	+INPUT	Analog input. Analog input positive connection.
11	V+	Positive power supply input.
12	D5	Digit drive output. Most Significant Digit (MSD)
13	B1	Binary Coded Decimal (BCD) output. Least Significant Bit (LSB)
14	B2	BCD output.
15	B4	BCD output.
16	B8	BCD output. Most Significant Bit (MSB)
17	D4	Digit drive output.
18	D3	Digit drive output.
19	D2	Digit drive output.
20	D1	Digit drive output. Least Significant Digit (LSD)
21	BUSY	Busy output. At the beginning of the signal-integration phase, BUSY goes High and remains High until the first clock pulse after the integrator zero crossing.
22	CLOCK IN	Clock input. Conversion clock connection.
23	POLARITY	Polarity output. A positive input is indicated by a logic High output. The polarity output is valid at the beginning of the reference integrate phase and remains valid until determined during the next conversion.
24	DGND	Digital logic reference input.
25	RUN/$\overline{\text{HOLD}}$	Run / Hold input. When at a logic High, conversions are performed continuously. A logic Low holds the current data as long as the Low condition exists.
26	$\overline{\text{STROBE}}$	Strobe output. The STROBE output pulses low in the center of the digit drive outputs.
27	OVERRANGE	Over range output. A logic High indicates that the analog input exceeds the full scale input range.
28	UNDERRANGE	Under range output. A logic High indicates that the analog input is less than 9% of the full scale input range.

3.0 DETAILED DESCRIPTION

(All Pin Designations Refer to 28-Pin DIP)

3.1 Dual Slope Conversion Principles

The TC835 is a dual slope, integrating analog to digital converter. An understanding of the dual slope conversion technique will aid in following the detailed TC835 operational theory.

The conventional dual slope converter measurement cycle has two distinct phases:

1. Input signal integration
2. Reference voltage integration (de-integration)

The input signal being converted is integrated for a fixed time period, with time being measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal.

In a simple dual slope converter, a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

A simple mathematical equation relates the input signal, reference voltage and integration time:

EQUATION 3-1:

$$\frac{1}{R_{INT}C_{INT}}\int_0^{T_{INT}} V_{IN}(T)DT = \frac{V_{REF}\,T_{DEINT}}{R_{INT}C_{INT}}$$

where:

V_{REF} = Reference voltage

T_{INT} = Signal integration time (fixed)

T_{DEINT} = Reference voltage integration time (variable).

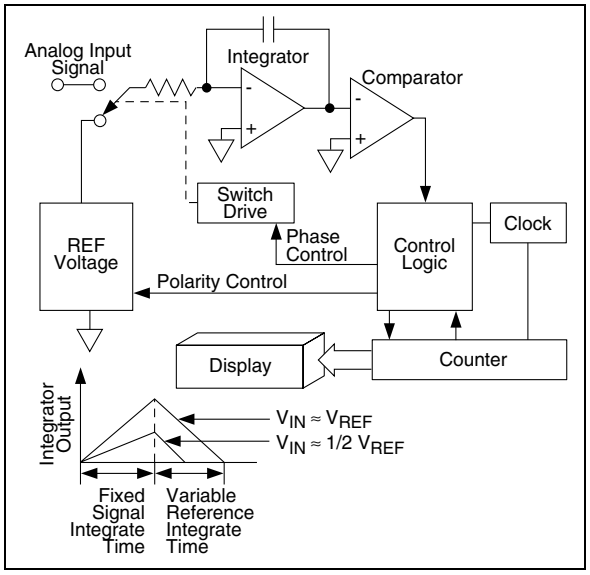
For a constant V_{IN}:

EQUATION 3-2:

$$V_{IN} = \frac{V_{REF}\,T_{DEINT}}{t_{INT}}$$

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated, or averaged, to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments (see Figure 3-1).

FIGURE 3-1: BASIC DUAL SLOPE CONVERTER



3.2 TC835 Operational Theory

The TC835 incorporates a system zero phase and integrator output voltage zero phase to the normal two phase dual slope measurement cycle. Reduced system errors, fewer calibration steps and a shorter overrange recovery time result.

The TC835 measurement cycle contains four phases:

1. System zero
2. Analog input signal integration
3. Reference voltage integration
4. Integrator output zero

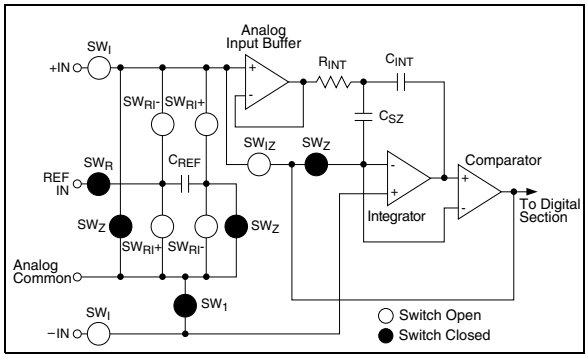
Internal analog gate status for each phase is shown in Table 3-1.

3.2.1 SYSTEM ZERO

During this phase, errors due to buffer, integrator and comparator offset voltages are compensated for by charging C_{AZ} (auto zero capacitor) with a compensating error voltage. With a zero input voltage the integrator output will remain at zero.

The external input signal is disconnected from the internal circuitry by opening the two SW_I switches. The internal input points connect to ANALOG COMMON. The reference capacitor charges to the reference voltage potential through SW_R. A feedback loop, closed around the integrator and comparator, charges the C_{AZ} capacitor with a voltage to compensate for buffer amplifier, integrator and comparator offset voltages (see Figure 3-2).

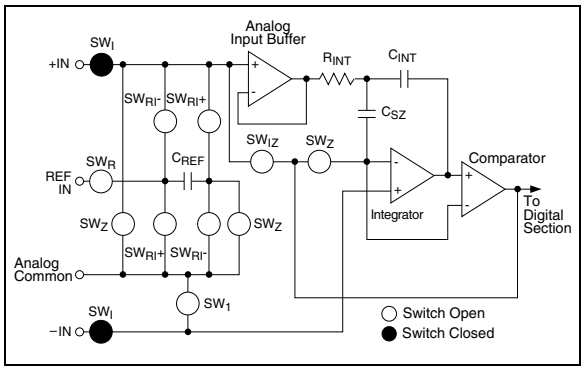
FIGURE 3-2: SYSTEM ZERO PHASE



3.2.2 ANALOG INPUT SIGNAL INTEGRATION

The TC835 integrates the differential voltage between the +INPUT and -INPUT pins. The differential voltage must be within the device Common mode range (-1V from either supply rail, typically). The input signal polarity is determined at the end of this phase (see Figure 3-3).

FIGURE 3-3: INPUT SIGNAL INTEGRATION PHASE

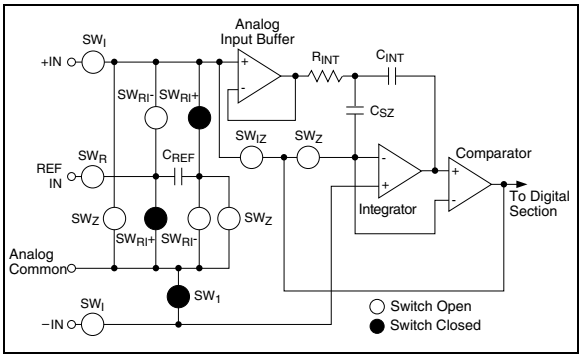


3.2.3 REFERENCE VOLTAGE INTEGRATION

The previously charged reference capacitor is connected with the proper polarity to ramp the integrator output back to zero (see Figure 3-4). The digital reading displayed is:

$$\text{Reading} = 10{,}000\ \frac{[\text{Differential Input}]}{V_{REF}}$$

FIGURE 3-4: REFERENCE VOLTAGE INTEGRATION CYCLE



3.2.4 INTEGRATOR OUTPUT ZERO

This phase guarantees the integrator output is at 0V when the system zero phase is entered and that the true system offset voltages are compensated for. This phase normally lasts 100 to 200 clock cycles. If an overrange condition exists, the phase is extended to 6200 clock cycles (see Figure 3-5).

FIGURE 3-5: INTEGRATOR OUTPUT ZERO PHASE

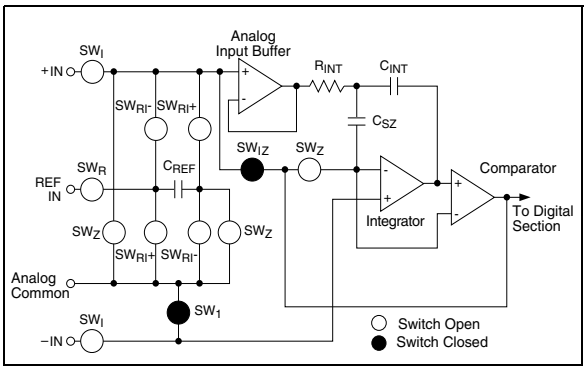


TABLE 3-1: INTERNAL ANALOG GATE STATUS

Conversion Cycle Phase	SW_I	$SW_{RI}+$	$SW_{RI}-$	SW_Z	SW_R	SW_1	SW_{IZ}	Reference Figures
System Zero				Closed	Closed	Closed		Figure 3-2
Input Signal Integration	Closed							Figure 3-3
Reference Voltage Integration		Closed*				Closed		Figure 3-4
Integrator Output Zero						Closed	Closed	Figure 3-5

***Note:** Assumes a positive polarity input signal. SW_{RI} would be closed for a negative input signal.

4.0 ANALOG SECTION FUNCTIONAL DESCRIPTION

(In Reference to the 28-Pin Plastic Package)

4.1 Differential Inputs (+INPUT (Pin 10) and –INPUT (Pin 9))

The TC835 operates with differential voltages within the input amplifier Common mode range. The input amplifier Common mode range extends from 0.5V below the positive supply to 1V above the negative supply. Within this Common mode voltage range, an 86dB Common mode rejection ratio is typical.

The integrator output also follows the Common mode voltage. The integrator output must not be allowed to saturate. An example of a worst case condition would be when a large positive Common mode voltage with a near full scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its swing has been used up by the positive Common mode voltage. For these critical applications, the integrator swing can be reduced to less than the recommended 4V full scale swing, with the effect of reduced accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

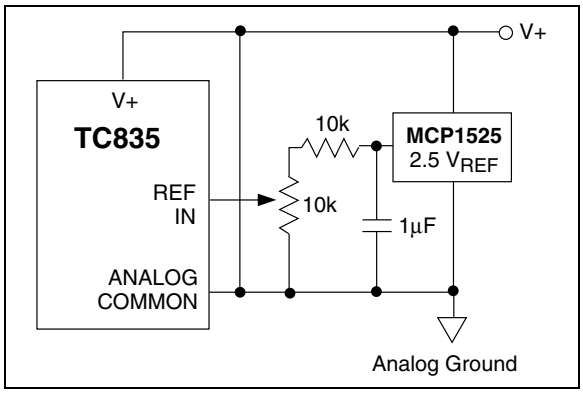
4.2 Analog Common Input (Pin 3)

ANALOG COMMON is used as the -INPUT return during auto zero and de-integrate. If -INPUT is different from ANALOG COMMON, a Common mode voltage exists in the system. This signal is rejected by the excellent CMRR of the converter. In most applications, -INPUT will be set at a fixed, known voltage (power supply common, for instance). In this application, ANALOG COMMON should be tied to the same point, thus removing the common-mode voltage from the converter. The reference voltage is referenced to ANALOG COMMON.

4.3 Reference Voltage Input (REF IN (Pin 2))

The REF IN input must be a positive voltage with respect to ANALOG COMMON. A reference voltage circuit is shown in Figure 4-1.

FIGURE 4-1: USING AN EXTERNAL REFERENCE



5.0 DIGITAL SECTION FUNCTIONAL DESCRIPTION

The major digital subsystems within the TC835 are illustrated in Figure 5-1, with timing relationships shown in Figure 5-2. The multiplexed BCD output data can be displayed on LCD or LED. The digital section is best described through a discussion of the control signals and data outputs.

FIGURE 5-1: DIGITAL SECTION FUNCTIONAL DIAGRAM

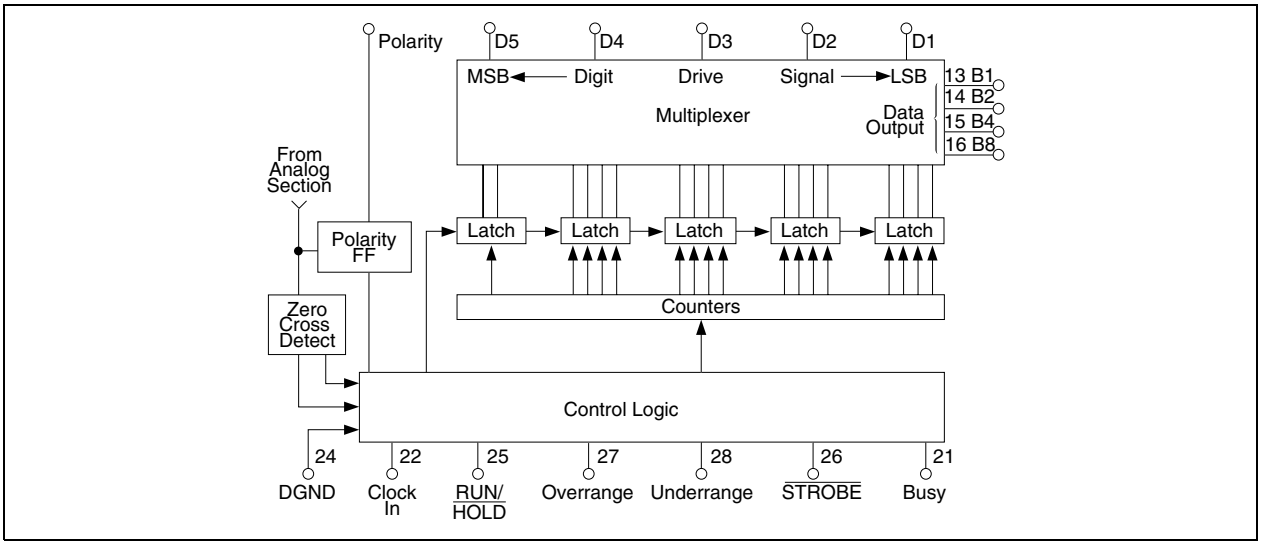
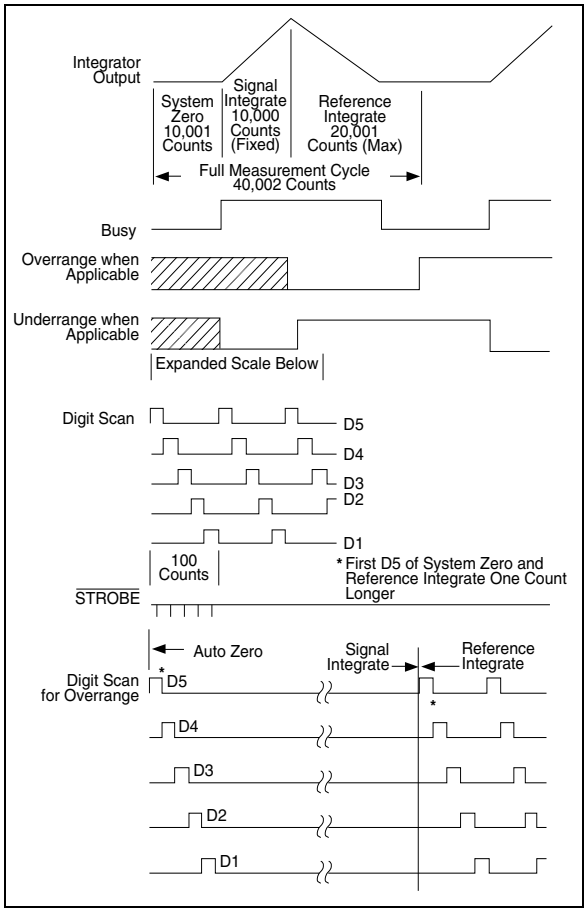


FIGURE 5-2: TIMING DIAGRAMS FOR OUTPUTS



5.1 RUN/HOLD Input (Pin 25)

When left open, this pin assumes a logic "1" level. With a RUN/HOLD = 1, the TC835 performs conversions continuously, with a new measurement cycle beginning every 40,002 clock pulses.

When RUN/HOLD changes to a logic "0," the measurement cycle in progress will be completed, and data held and displayed as long as the logic "0" condition exists.

A positive pulse (>300nsec) at RUN/HOLD initiates a new measurement cycle. The measurement cycle in progress when RUN/HOLD initially assumed the logic "0" state must be completed before the positive pulse can be recognized as a single conversion run command.

The new measurement cycle begins with a 10,001-count auto zero phase. At the end of this phase, the busy signal goes high.

5.2 STROBE Output (Pin 26)

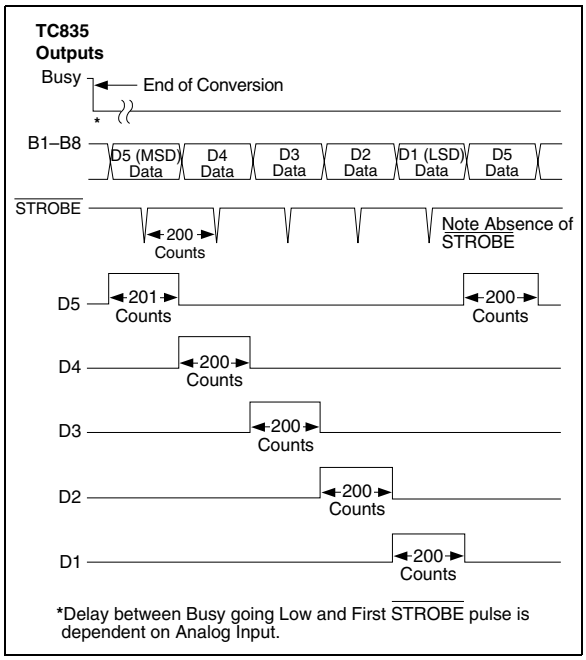
During the measurement cycle, the STROBE control line is pulsed low five times. The five low pulses occur in the center of the digit drive signals (D_1, D_2, D_3, D_5) (see Figure 5-3).

D_5 (MSD) goes high for 201 counts when the measurement cycles end. In the center of the D_5 pulse, 101 clock pulses after the end of the measurement cycle, the first STROBE occurs for one-half clock pulse. After the D_5 digit strobe, D_4 goes high for 200 clock pulses. The STROBE goes low 100 clock pulses after D_4 goes high. This continues through the D_1 digit drive pulse.

The digit drive signals will continue to permit display scanning. STROBE pulses are not repeated until a new measurement is completed. The digit drive signals will not continue if the previous signal resulted in an overrange condition.

The active low STROBE pulses aid BCD data transfer to UARTs, processors and external latches.

FIGURE 5-3: STROBE SIGNAL LOW FIVE TIMES PER CONVERSION



5.3 BUSY Output

At the beginning of the signal integration phase, BUSY goes high and remains high until the first clock pulse after the integrator zero crossing. BUSY returns to the logic "0" state after the measurement cycle ends in an overrange condition. The internal display latches are loaded during the first clock pulse after BUSY and are latched at the clock pulse end. The BUSY signal does not go high at the beginning of the measurement cycle, which starts with the auto zero cycle.

5.4 OVERRANGE Output

If the input signal causes the reference voltage integration time to exceed 20,000 clock pulses, the OVERRANGE output is set to a logic "1." The overrange output register is set when BUSY goes low, and is reset at the beginning of the next reference integration phase.

5.5 UNDERRANGE Output

If the output count is 9% of full scale or less (-1800 counts), the underrange register bit is set at the end of BUSY. The bit is set low at the next signal integration phase.

5.6 POLARITY Output

A positive input is registered by a logic "1" polarity signal. The POLARITY bit is valid at the beginning of Reference Integrate and remains valid until determined during the next conversion.

The POLARITY bit is valid even for a zero reading. Signals less than the converter's LSB will have the signal polarity determined correctly. This is useful in null applications.

5.7 Digit Drive Outputs

Digit drive signals are positive going signals. The scan sequence is D_5 to D_1. All positive pulses are 200 clock pulses wide, except D_5, which is 201 clock pulses wide.

All five digits are scanned continuously, unless an overrange condition occurs. In an overrange condition, all digit drives are held low from the final STROBE pulse until the beginning of the next reference integrate phase. The scanning sequence is then repeated. This provides a blinking visual display indication.

5.8 BCD Data Outputs

The binary coded decimal (BCD) bits B_8, B_4, B_2, B_1 are positive-true logic signals. The data bits become active simultaneously with the digit drive signals. In an overrange condition, all data bits are at a logic "0" state.

6.0 TYPICAL APPLICATIONS

6.1 Component Value Selection

The integrating resistor is determined by the full-scale input voltage and the output current of the buffer used to charge the integrator capacitor. Both the buffer amplifier and the integrator have a class A output stage, with 100µA of quiescent current. A 20µA drive current gives negligible linearity errors. Values of 5µA to 40µA give good results. The exact value of an integrating resistor for a 20µA current is easily calculated.

EQUATION 6-1:

$$R_{INT} = \frac{\text{Full scale voltage}}{20\mu A}$$

6.1.1 INTEGRATING CAPACITOR

The product of integrating resistor and capacitor should be selected to give the maximum voltage swing that ensures the tolerance buildup will not saturate the integrator swing (approximately 0.3V from either supply). For ±5V supplies and ANALOG COMMON tied to supply ground, a ±3.5V to ±4V full-scale integrator swing is adequate. A 0.10µF to 0.47µF is recommended. In general, the value of C_{INT} is given by:

EQUATION 6-2:

$$C_{INT} = \frac{[10{,}000 \times \text{clock period}] \times I_{INT}}{\text{Integrator output voltage swing}}$$

$$= \frac{(10{,}000)\ (\text{clock period})\ (20\mu A)}{\text{Integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor is that it has low dielectric absorption to prevent rollover or ratiometric errors. A good test for dielectric absorption would be to use the capacitor with the input tied to the reference. This ratiometric condition should read half scale 0.9999, with any deviation probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

6.1.2 AUTO ZERO AND REFERENCE CAPACITORS

The size of the auto zero capacitor has some influence on the noise of the system. A large capacitor reduces the noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

The dielectric absorption of the reference capacitor and auto zero capacitor are only important at power-on or when the circuit is recovering from an overload.

Smaller or cheaper capacitors can be used if accurate readings are not required for the first few seconds of recovery.

6.1.3 REFERENCE VOLTAGE

The analog input required to generate a full scale output is $V_{IN} = 2V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. For this reason, it is recommended that a high-quality reference be used where high-accuracy absolute measurements are being made.

6.2 Conversion Timing

6.2.1 LINE FREQUENCY REJECTION

A signal integration period at a multiple of the 60Hz line frequency will maximize 60Hz "line noise" rejection. A 200kHz clock frequency will reject 60Hz and 400Hz noise. This corresponds to five readings per second (see Table 6-1 and Table 6-2).

TABLE 6-1: CONVERSION RATE VS. CLOCK FREQUENCY

Oscillator Frequency (kHz)	Conversion Rate (Conv./Sec.)
100	2.5
120	3
200	5
300	7.5
400	10
800	20
1200	30

TABLE 6-2: LINE FREQUENCY VS. CLOCK FREQUENCY

Oscillator Frequency (kHz)	Line Frequency Rejection		
	60Hz	50Hz	400Hz
50.000	•	•	•
53.333	—	—	•
66.667	•	—	•
80.000	—	—	•
83.333	—	•	•
100.000	•	•	•
125.000	—	•	•
133.333	—	—	•
166.667	—	—	•
200.000	•	—	•
250.000			

The conversion rate is easily calculated:

EQUATION 6-3:

$$\text{Reading 1/sec} = \frac{\text{Clock Frequency (Hz)}}{4000}$$

6.3 Power Supplies and Grounds

6.3.1 POWER SUPPLIES

The TC835 is designed to work from ±5V supplies. For single +5V operation, a TC7660 can provide a –5V supply.

6.3.2 GROUNDING

Systems should use separate digital and analog ground systems to avoid loss of accuracy.

6.4 High-Speed Operation

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. The comparator in this circuit follows the integrator ramp with a 3µsec delay, and at a clock frequency of 200kHz (5µsec period), half of the first reference integrate clock period is lost in delay. This means that the meter reading will change from 0 to 1 with a 50µV input, 1 to 2 with 150µV, 2 to 3 at 250µV, etc. This transition at midpoint is considered desirable by most users, however, if the clock frequency is increased appreciably above 200kHz, the instrument will flash "1" on noise peaks even when the input is shorted.

For many dedicated applications where the input signal is always of one polarity, the delay of the comparator need not be a limitation. Since the nonlinearity and noise do not increase substantially with frequency, clock rates of up to ~1MHz may be used. For a fixed clock frequency, the extra count or counts caused by comparator delay will be a constant and can be subtracted out digitally.

The clock frequency may be extended above 200kHz without this error, however, by using a low-value resistor in series with the integrating capacitor. The effect of the resistor is to introduce a small pedestal voltage onto the integrator output at the beginning of the reference integrate phase. By careful selection of the ratio between this resistor and the integrating resistor (a few tens of ohms in the recommended circuit), the comparator delay can be compensated and the maximum clock frequency extended by approximately a factor of 3. At higher frequencies, ringing and second-order breaks will cause significant nonlinearities in the first few counts of the instrument.

The minimum clock frequency is established by leakage on the auto zero and reference capacitors. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

The clock used should be free from significant phase or frequency jitter. Several suitable low-cost oscillators are shown in Section 6.0, Typical Applications. The multiplexed output means that if the display takes significant current from the logic supply, the clock should have good PSRR.

6.5 Zero Crossing Flip-Flop

The flip flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. False zero crossings caused by clock pulses are not recognized. Of course, the flip flop delays the true zero crossing by up to one count in every instance. If a correction were not made, the display would always be one count too high.

Therefore, the counter is disabled for one clock pulse at the beginning of the reference integrate (de-integrate) phase. This one-count delay compensates for the delay of the zero crossing flip flop and allows the correct number to be latched into the display. Similarly, a one-count delay at the beginning of auto zero gives an overload display of 0000 instead of 0001. No delay occurs during signal integrate, so that true ratiometric readings result.

FIGURE 6-1: 4-1/2 DIGIT ADC MULTIPLEXED COMMON ANODE LED DISPLAY

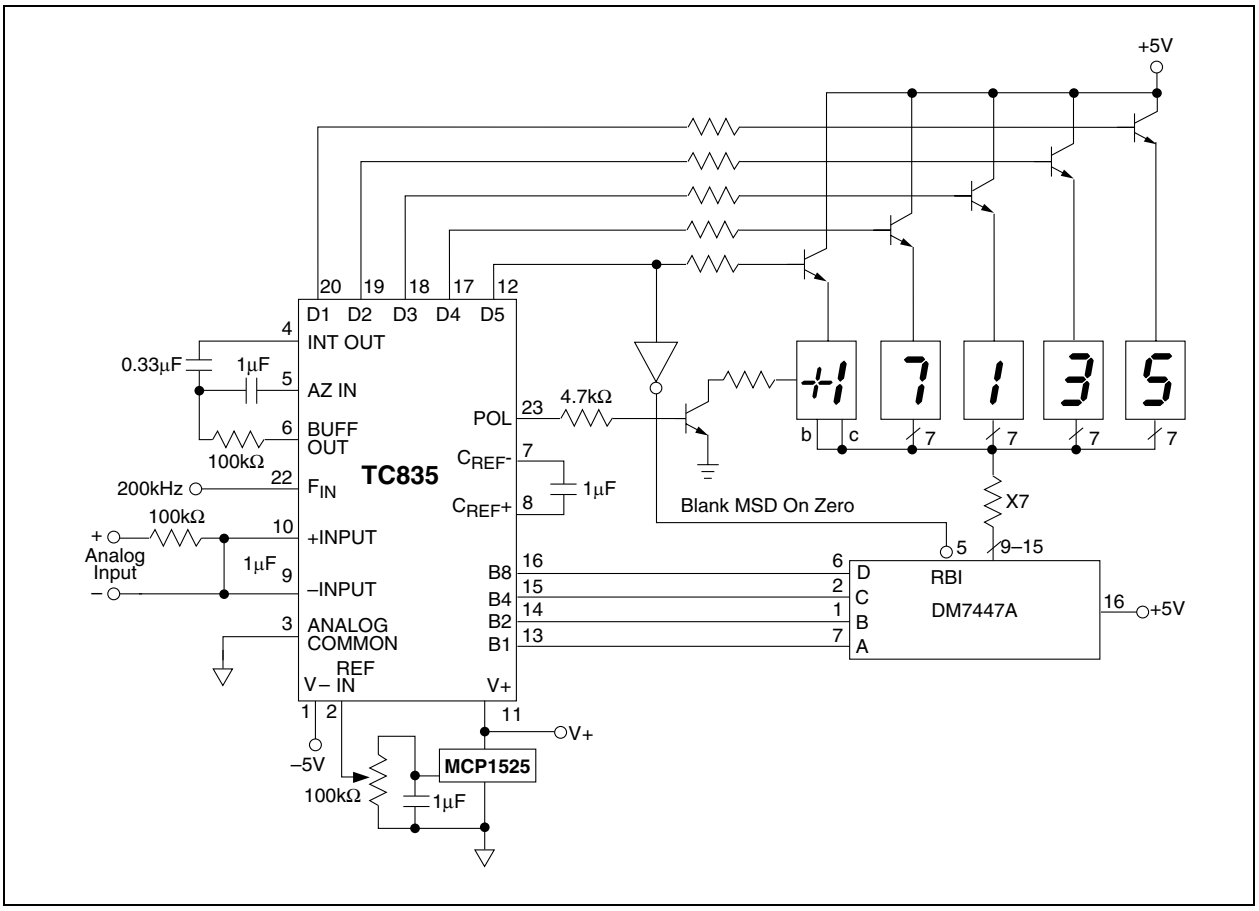
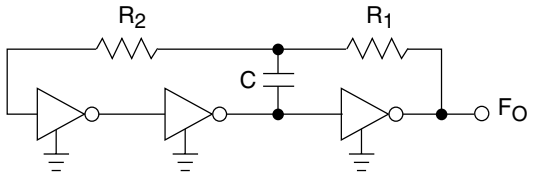


FIGURE 6-2: RC OSCILLATOR CIRCUIT



Gates are 74C04

1. $f_O = \frac{1}{2C(0.41R_P + 0.7R_1)}$, $R_P = \frac{R_1 R_2}{R_1 + R_2}$

   a. If $R_1 = R_2 = R_1$, $F \cong 0.55/RC$

   b. If $R_2 >> R_1$, $f \cong 0.45/R_1C$

   c. If $R_2 << R_1$, $f \cong 0.72/R_1C$

2. Examples:

   a. f = 120kHz, C = 420pF
   $R_1 = R_2 \approx 10.9k\Omega$

   b. f = 120kHz, C = 420pF, $R_2 = 50k\Omega$
   $R_1 = 8.93k\Omega$

   c. f = 120kHz, C = 220pF, $R_2 = 5k\Omega$
   $R_1 = 27.3k\Omega$

FIGURE 6-3: COMPARATOR CLOCK CIRCUITS

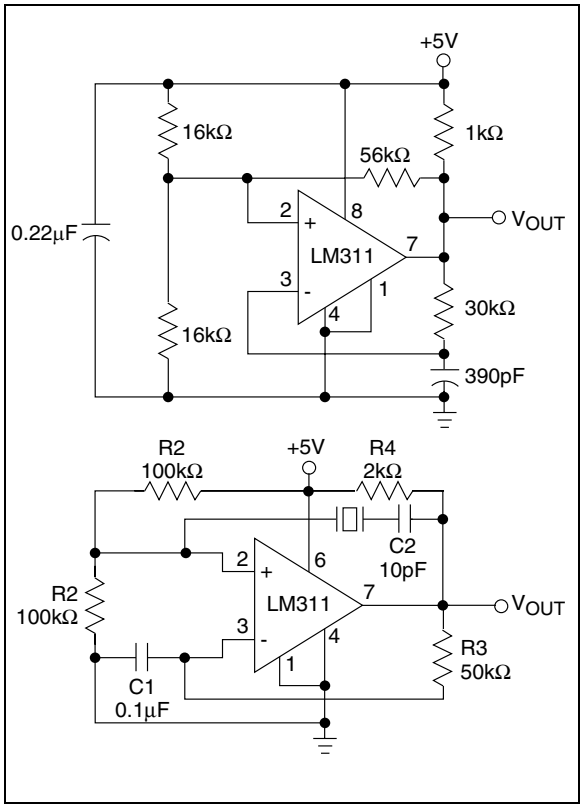


FIGURE 6-4: 4-1/2 DIGIT ADC WITH MULTIPLEXED COMMON CATHODE LED DISPLAY

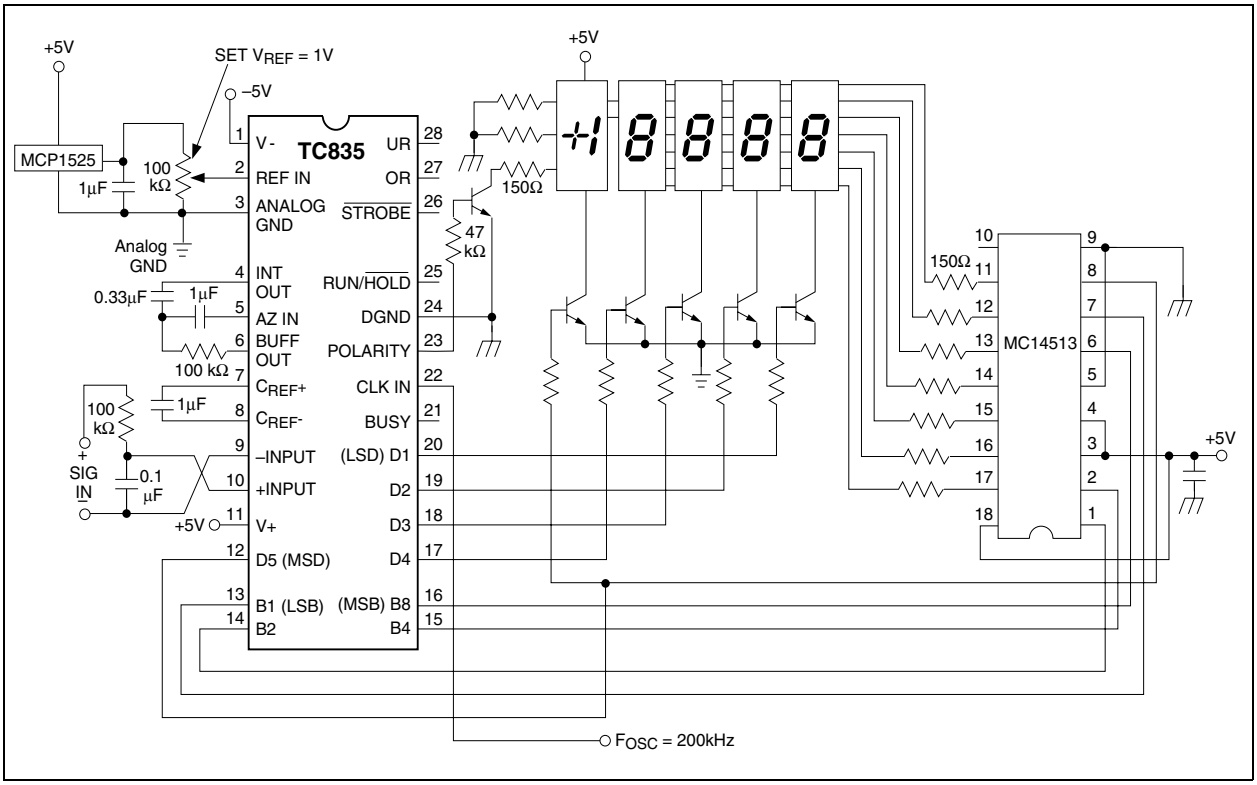
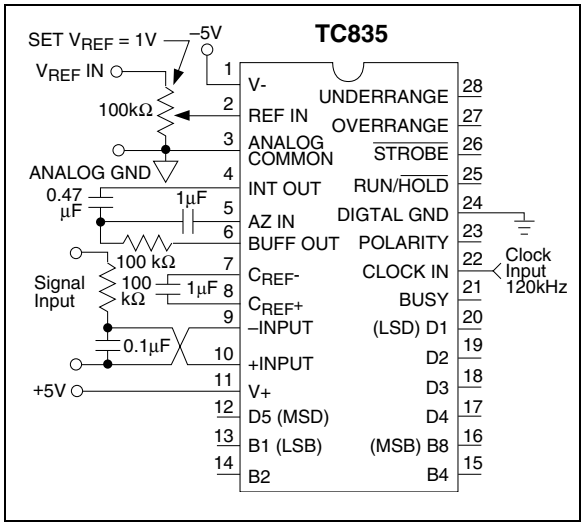


FIGURE 6-5: TEST CIRCUIT



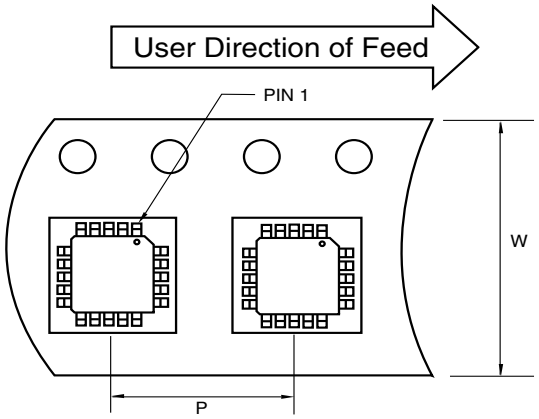
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

Package marking data not available at this time.

7.2 Taping Forms

Component Taping Orientation for 64-Pin PQFP Devices



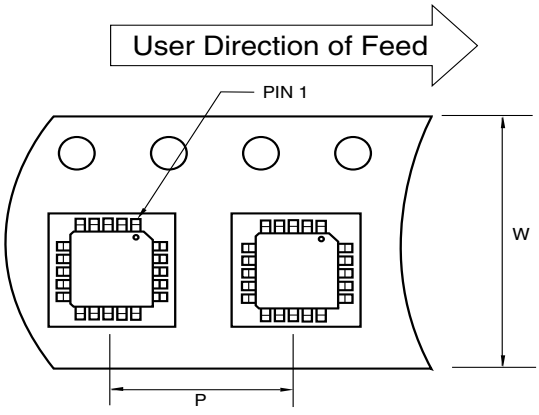
Standard Reel Component Orientation
for TR Suffix Device

Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
64-Pin PQFP	32 mm	24 mm	250	13 in

NOTE: Drawing does not represent total number of pins.

Component Taping Orientation for 44-Pin PQFP Devices



Standard Reel Component Orientation
for TR Suffix Device

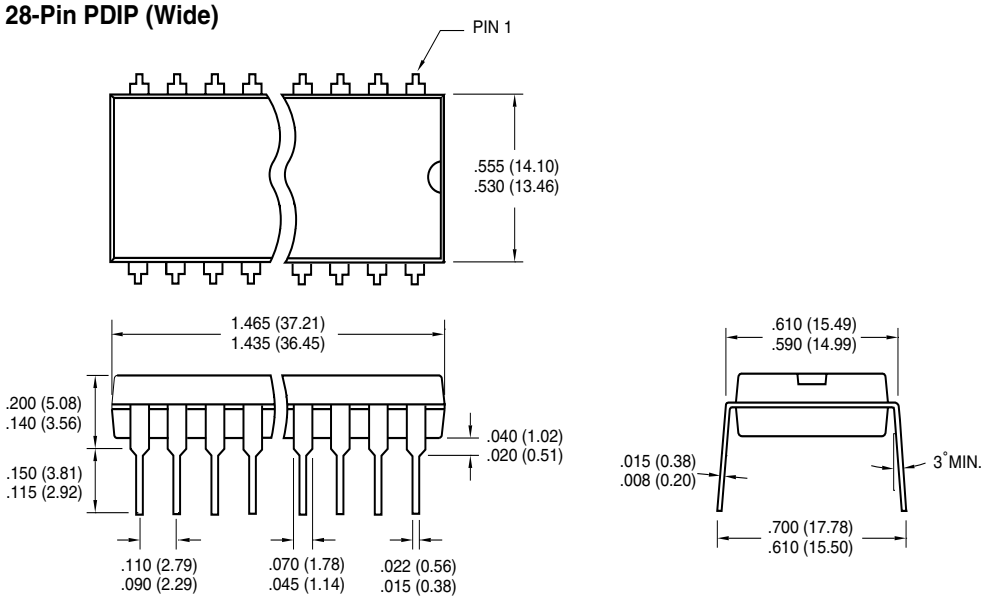
Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
44-Pin PQFP	24 mm	16 mm	500	13 in

NOTE: Drawing does not represent total number of pins.

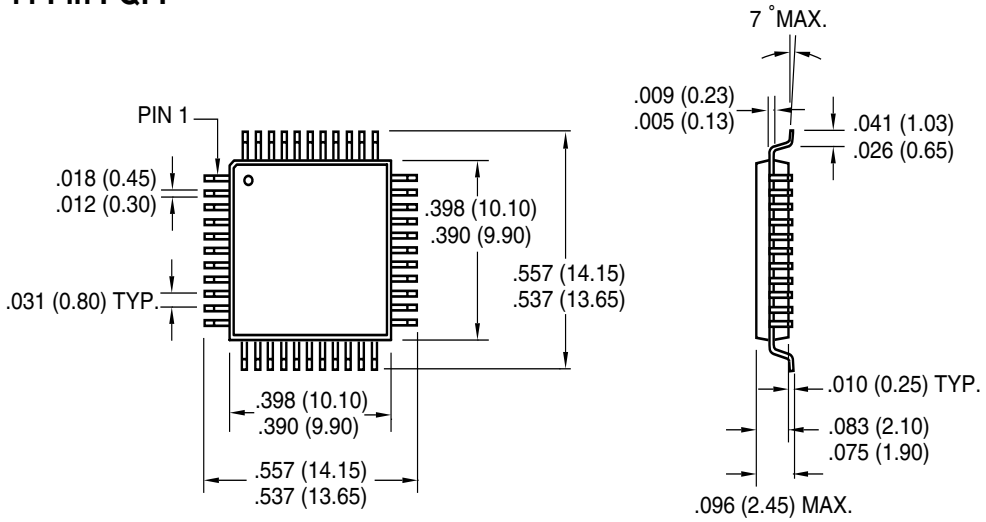
7.3 Package Dimensions

28-Pin PDIP (Wide)



Dimensions: inches (mm)

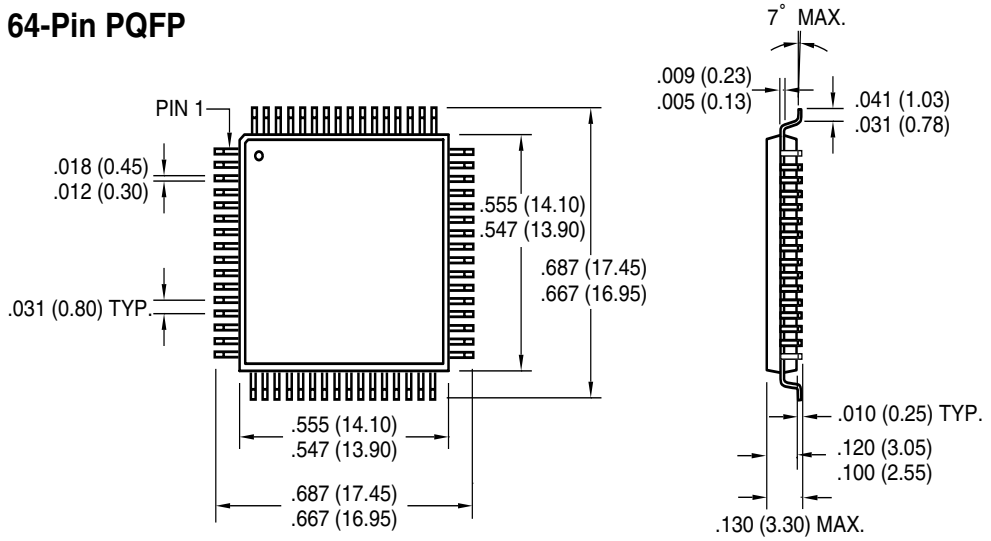
44-Pin PQFP



Dimensions: inches (mm)

7.3 Package Dimensions (Continued)

64-Pin PQFP



Dimensions: inches (mm)

NOTES:

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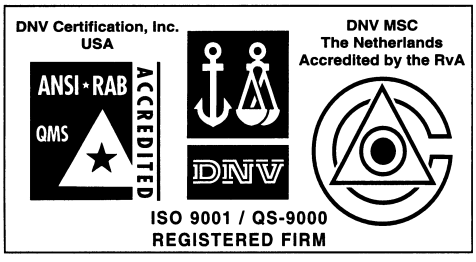

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