

Features

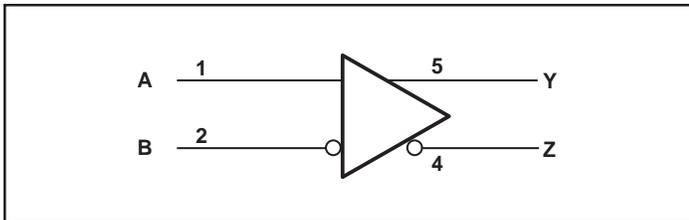
- Complies with ANSI/TIA/EIA-644-A LVDS standard
- LVDS receiver inputs accept LVPECL signals
- Low jitter 660 Mbps fully differential data path
- Bus-Terminal ESD exceeds 2kV
- Single +3.3 V supply voltage operation
- Receiver Differential Input Voltage Threshold $< \pm 100$ mV
- Receiver open-circuit failsafe
- Low-Voltage Differential Signaling with typical Output Voltages of 350mV into:
 - 100-ohm Load (PI90LV03)
 - 50-ohm Load (PI90LVB03)
- Typical Propagation Delay Times of 1.5ns
- Typical Power Dissipation of 20mW @ 200MHz
- Outputs are High Impedance with $V_{CC} < 1.5V$
- Industrial Temperature Range: $-40^{\circ}C$ to $85^{\circ}C$
- Package: 6-pin space-saving SOT-23 (T)

Function Table

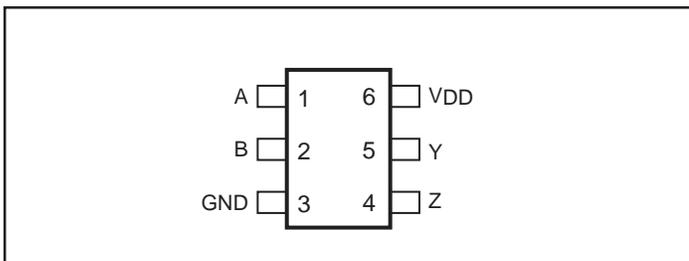
Inputs	Outputs
$V_{ID} = V_A - V_B$	$V_Y - V_Z$
$V_{ID} > 50mV$	H
$-50mV < V_{ID} < 50mV$?
$V_{ID} \leq -50mV$	L
Open	H

H = high level; L = low level; ? = indeterminate

Logic Diagram



Pinout



Description

PI90LV03 and PI90LVB03 are single LVDS Repeaters that use low-voltage differential signaling (LVDS) to support data rates up to 660 Mbps. The PI90LVB03 features high-drive output. These products are designed for applications requiring high-speed, low-power consumption, low-noise generation, and a small package.

The LVDS Repeaters take an LVDS input signal and provide an LVDS output to address various interface logic requirements such as signal isolation, repeater, stub length, and Optical Transceiver Modules. In many large systems, signals are distributed across backplanes, and the distance between the transmission line and the unterminated receivers are one of the limiting factors for system speed. The buffers can be used to reduce the ‘stub length’ by strategic device placement along the trace length. They can improve system performance by allowing the receiver to be placed very close to the main transmission line or very close to the connector on the card. Longer traces to the LVDS receiver can then be placed after the buffer.

The buffer’s wide input dynamic range enables them to receive differential signals from LVPECL and LVDS sources. The devices can be used as compact high-speed serial translators between LVPECL and LVDS data lines. The differential translation provides a simple way to mix and match Optical Transceiver ICs from various vendors without redesigning the interfaces.

Applications

The PI90LV03 and PI90LVB03 provide differential translation between LVDS and PECL devices for high-speed, point-to-point interface and telecom applications:

- ATM
- SONET/SDH
- Switches
- Routers
- Add-Drop Multiplexers

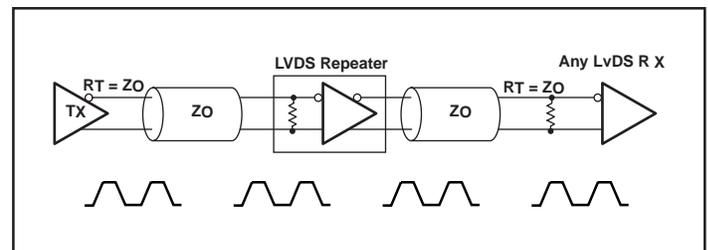


Figure 1. High-Speed Differential Cable Repeater Application

Absolute Maximum Ratings Over Operating Free-Air Temperature

(unless otherwise noted)†

Supply Voltage Range, $V_{CC}^{(1)}$	-0.5V to 4V	Continuous total power dissipation ...	See dissipation rating table
Voltage Range (A, B, or R_{OUT})	-0.5 to $V_{CC}+0.5V$	Storage Temperature Range	-65°C to 150°C
ESD rating (HBM, 1.5k-ohms, 100pF)	≥2KV	Lead Temperature 1.6 mm (1/16 inch) from case for 10 seconds	250°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability.

Notes:

1. All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

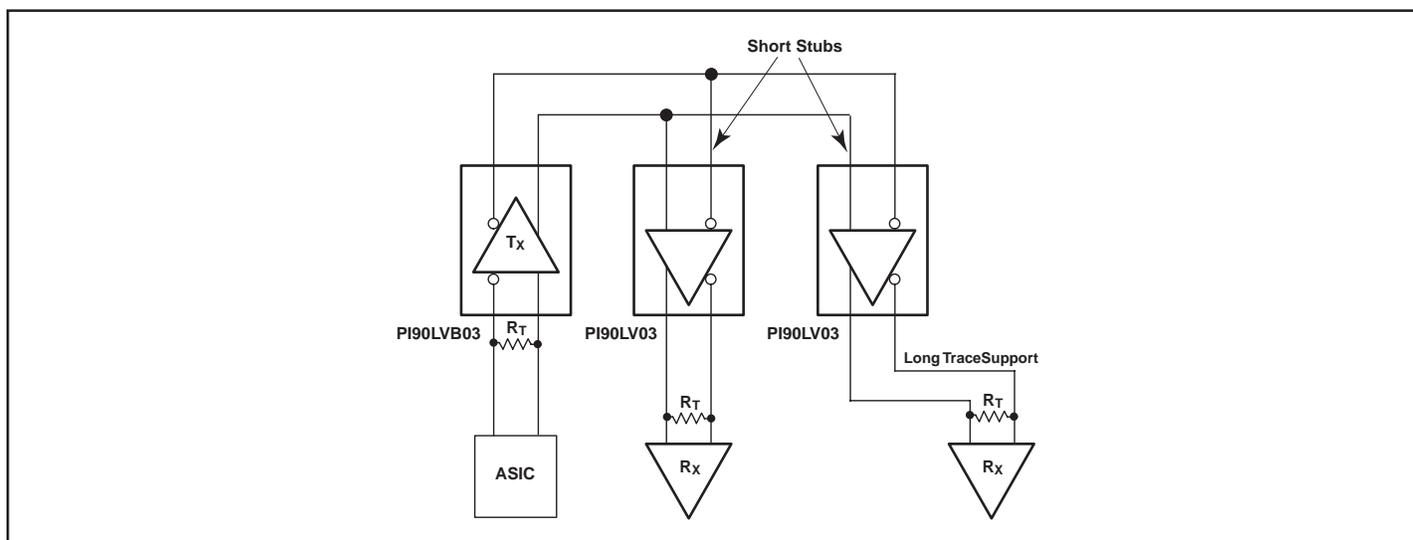


Figure 2. Backplane Stub-Hider Application

Dissipation Rating Table

Package	$T_A \leq 25^\circ\text{C}$ Power Rating	Derating Factor Above $T_A = 25^\circ\text{C}^{*}$	$T_A = 85^\circ\text{C}$ Power Rating
6-Pin SOT (T)	385mW	3.1mW/°C	200mW

*This is the inverse of the junction-to-ambient thermal resistance when board-mounted (low-K) and with no air flow.

Recommended Operating Conditions

	Min.	Nom.	Max.	Units
Supply Voltage, V_{CC}	3.0	3.3	3.6	V
Magnitude of differential input voltage, $ V_{ID} $	0.1		0.6	
Common-Mode Input Voltage, V_{IC} (See Figure 6)	0		$2.0 - \frac{ V_{ID} }{2}$ $V_{CC} - 0.8$	
Operating free-air temperature, T_A	-40		85	°C

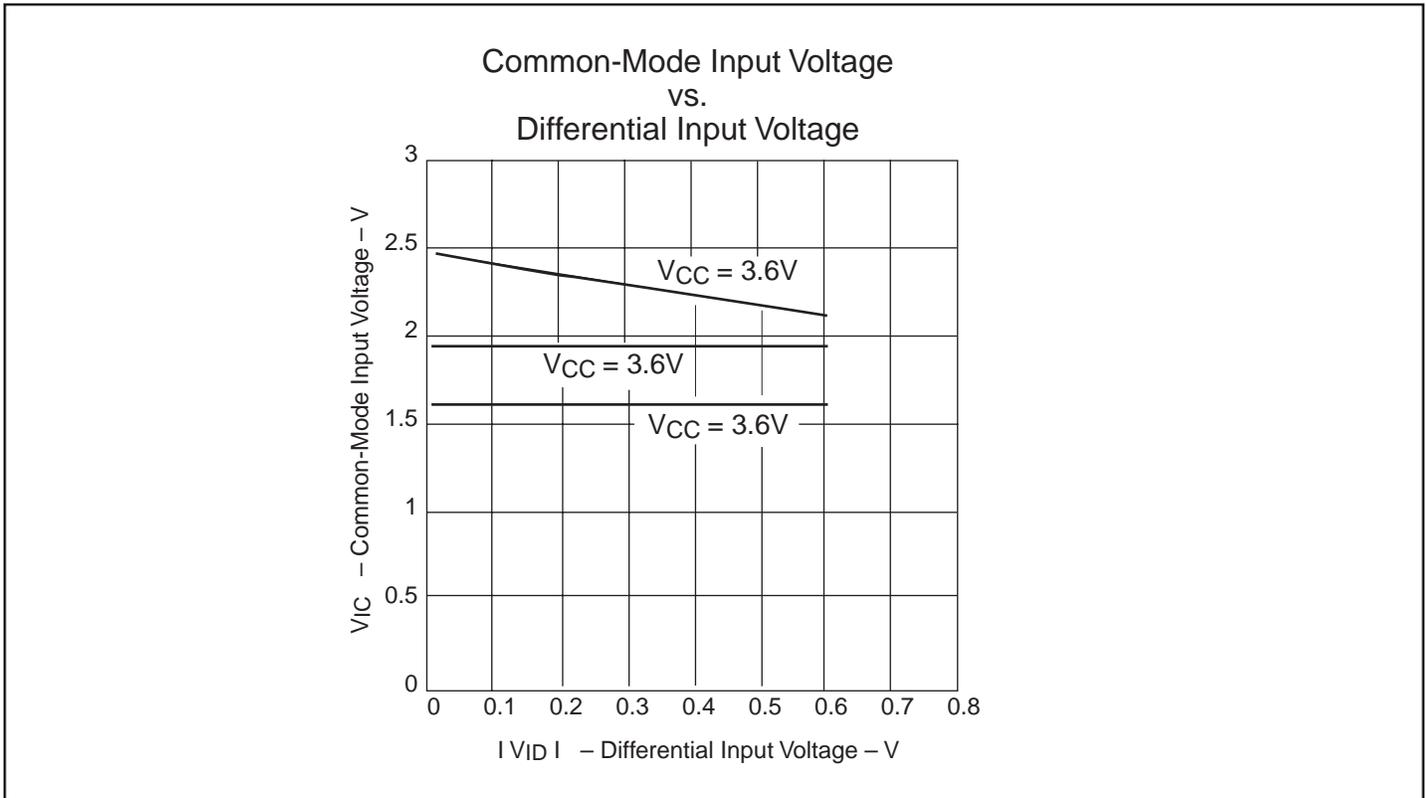


Figure 3. V_{IC} vs. V_{ID} and V_{CC}

Note: 1. All typical values are at 25°C and with a 3.3V supply.

Electrical Characteristics over Recommended Operating Conditions (unless otherwise noted).

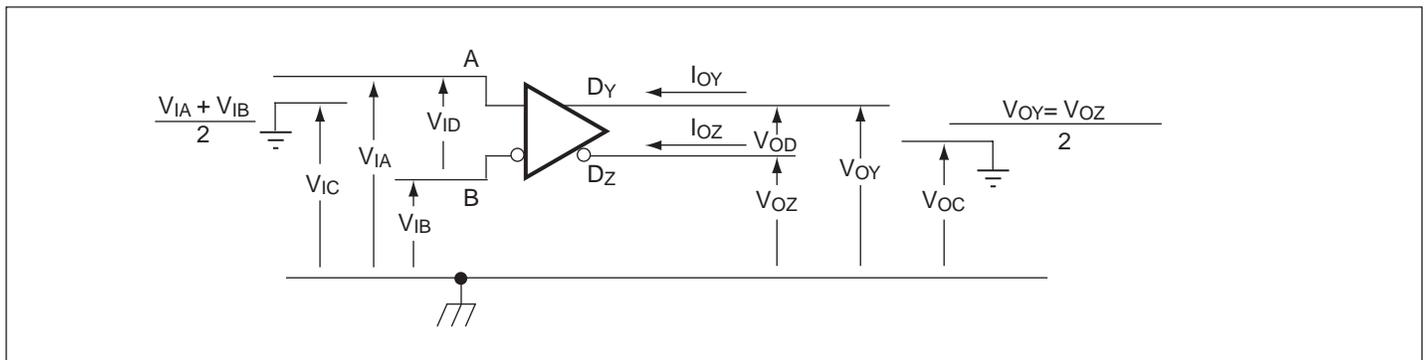
Symbol	Parameter	Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Units	
V _{ITH+}	Positive-going differential input voltage threshold	See Figure 4, & Table 1			50	mV	
V _{ITH-}	Negative-going differential input voltage threshold		-50				
I _I	Input current (A or B inputs)	V _I = 0V			±20	μA	
		V _I = 2.4V or V _{CC} -0.8	-1.2				
I _{ID}	High-level input current (I _{IA} - I _{IB})	V _{IA} = 0V, V _{IB} = 0.1V V _{IA} = 2.4V, V _{IB} = 2.3V			±2		
V _{OD}	Differential output voltage magnitude	R _L = 100-ohms (LV03); R _L = 50-ohms (LVB03) See Figure 4	247	350	454	mV	
Δ V _{OD}	Change in differential output voltage magnitude between logic states		-50		50		
V _{OC(SS)}	Steady-state common-mode output voltage	See Figure 5	1.125		1.375	V	
ΔV _{OC(SS)}	Change in steady-state common-mode output voltage between logic states		-50		50	mV	
V _{OC(PP)}	Peak-to-peak common-mode output voltage			25	100		
I _{CC}	Supply Current	V _I = 0V or V _{CC} , No load		7	9	mA	
		V _I = 0V or V _{CC} , R _L = 100-ohms (LV03)		9.5	12.5		
		V _I = 0V or V _{CC} , R _L = 50-ohms (LVB03)		18	25		
I _{OS}	Short-circuit output current	V _{OY} or V _{OZ} = 0V	LV03		3	10	mA
			LVB03		6	20	
I _{OS}	Short-circuit output current	V _{OD} = 0V	LV03			10	mA
			LVB03			20	
I _{O(OFF)}	Power-off output current	V _{CC} = 0V, V _O = 3.6V			±1	μA	
C _I	Input load capacitance			3		pF	

Receiver Switching Characteristics over Recommended Operating Conditions, (unless otherwise noted).

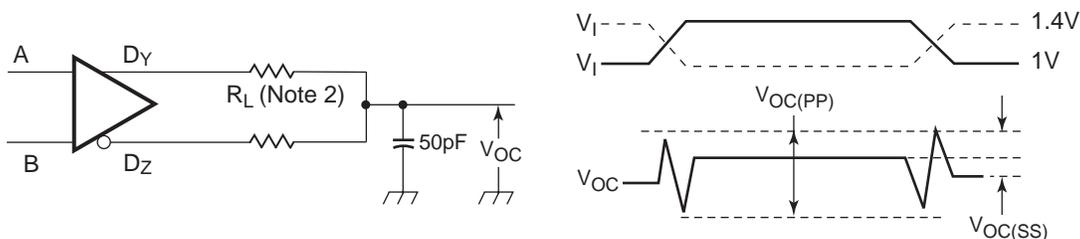
Symbol	Parameter	Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Units
t_{PLH}	Propagation delay time, low-to-high level output	PI90LV03, $R_L = 100$ ohms PI90LVB03, $R_L = 50$ ohms $C_L = 10$ pF, See Figure 6		1.4	6	ns
t_{PHL}	Propagation delay time, high-to-low level output			1.4	6	
t_r	Output signal rise time			0.5	1	
t_f	Output signal fall time			0.5	1	
$t_{sk(p)}$	Pulse skew ($ t_{PHL} - t_{PLH} $) ⁽²⁾			50		ps
t_{skpp}	Part-to-part skew			1.5		ns
f_{max}	Maximum throughput data rate ⁽³⁾			660		mbps

Notes:

- All typical values are at 25°C and with a 3.3V supply
- $t_{sk(p)}$ is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.
- f_{max} generator input conditions: 50% duty cycle, 200mV, Output criteria: 45% to 55% duty cycle, $V_{OD} \geq 250$ mV

Parameter Measurement Information

Figure 4. Voltage Definitions
Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

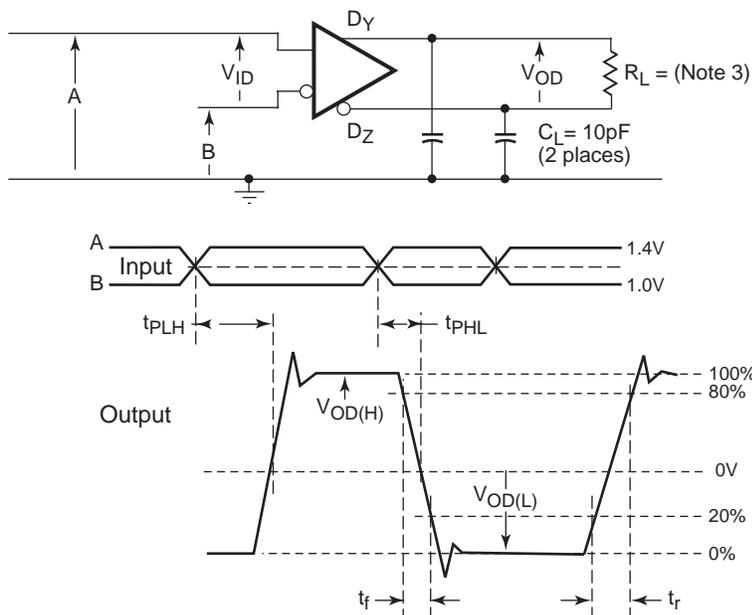
Applied Voltages (V)		Resulting Differential Input Voltage (mV)	Resulting Common-Mode Input Voltage (V)
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25	1.20	50	1.2
1.15	1.20	-50	1.2
2.4	2.35	50	2.35
2.3	2.35	-50	2.35
0.05	0	50	0.05
0	0.05	-50	0.05
1.5	0.9	600	1.2
0.9	1.5	-600	1.2
2.4	1.8	600	2.1
1.8	2.4	-600	2.1
0.6	0	600	0.3
0	0.6	-600	0.3



Notes:

1. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1\text{ns}$, Pulse Repetition Rate (PPR) = 0.5 Mpps, pulse width = $500 \pm 10\text{ns}$. C_L includes instrumentation and fixture capacitance within 0.06m of the D.U.T. The test measurement of $V_{OC(PP)}$ is made on test equipment with a -3dB bandwidth of at least 300MHz.
2. $R_L = 49.9\text{ohms} \pm 1\%$ for PI90LV03 or $24.9\text{ohms} \pm 1\%$ for PI90LVB03.
3. To verify output max signaling rate, the output signal transition time (t_r/t_f) should not exceed 0.76ns.

Figure 5. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

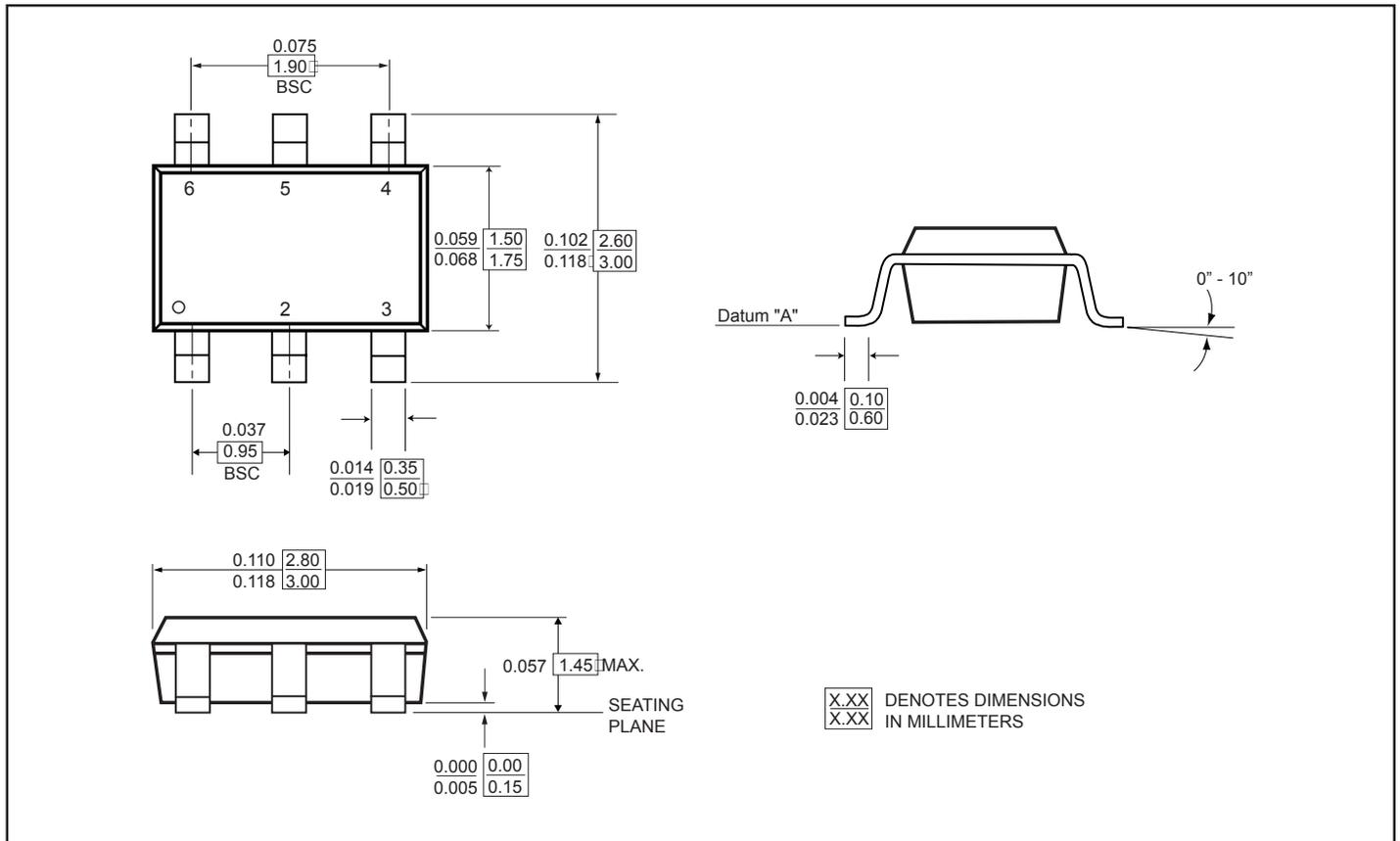


Notes:

1. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1\text{ns}$, Pulse Repetition Rate (PPR) = 50 Mpps, pulse width = $10 \pm 0.2\text{ns}$. C_L includes instrumentation and fixture capacitance within 0.06m of the D.U.T.
2. This point is 1.4V with $V_{CC} = 3.3\text{V}$ or 1.2V with $V_{CC} = 2.7\text{V}$.
3. $R_L = 100\text{ohms} \pm 1\%$ for PI90LV03 or $50\text{ohms} \pm 1\%$ for PI90LVB03.

Figure 6. Test Circuit and Definitions

6-Pin SOT Package (T)



Ordering Information

Part	Top mark	Pin - Package	Temperature
PI90LV03T	B03	6-Pin SOT23	-40°C to 85°C
PI90LVB03T	BB3	6-Pin SOT23	