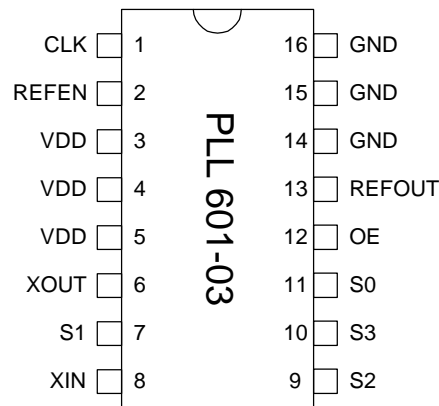


## Low Phase Noise PLL Clock Multiplier

### FEATURES

- Full swing CMOS outputs with 25 mA drive capability at TTL levels.
- Reference 10-30MHz crystal or clock.
- Integrated crystal load capacitor: no external load capacitor required.
- Output clocks up to 198MHz at 3.3V.
- Low phase noise ( $-126\text{dBc/Hz}$  @ 1kHz).
- Output Enable function.
- Low jitter (RMS): 6.4ps (period), 9.4ps (accum.)
- Advanced low power sub-micron CMOS process.
- 3.3V operation.
- Available in 16-Pin SOIC or TSSOP.

### PIN CONFIGURATION



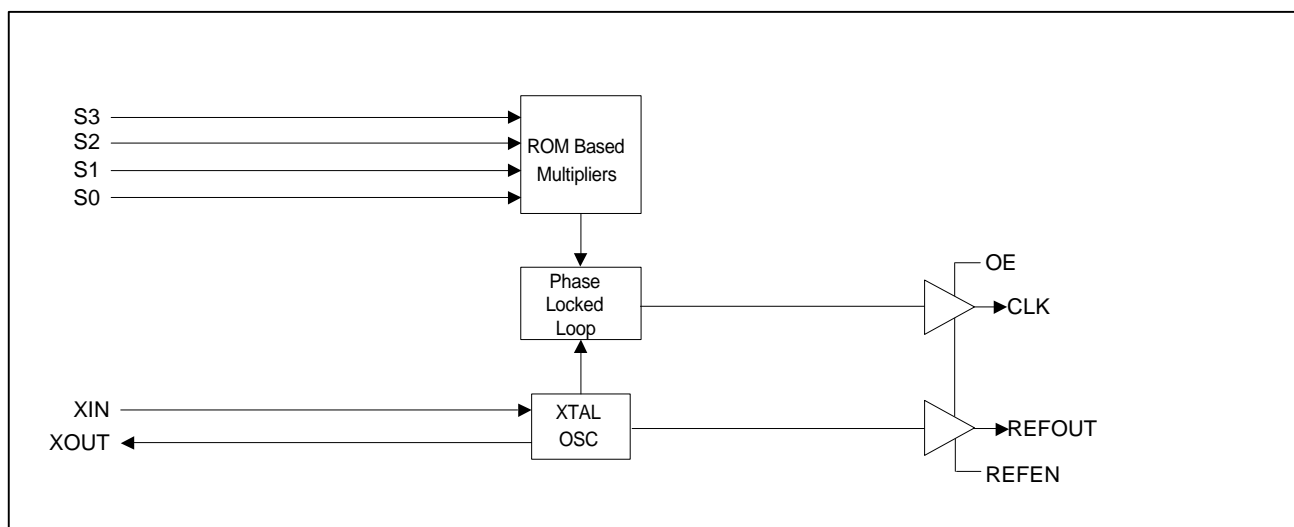
### DESCRIPTIONS

The PLL601-03 is a low cost, high performance and low phase noise clock synthesizer. It implements PhaseLink's proprietary analog and digital Phase Locked Loop techniques to allow the user to select the desired multiplier value. The chip accepts crystal or clock inputs ranging from 10 to 30MHz, depending on selected multiplier, and produces outputs clocks up to 198MHz at 3.3V.

### MULTIPLIER SELECT TABLE

S3	S2	S1	S0	Multiplier	Xtal range
0	0	0	0	Reserved	
0	0	0	1	11x	10-18MHz
0	1	0	1	5x	20-30MHz
1	0	0	1	Frequency Pass through	
1	1	0	1	6x	11-22MHz

### BLOCK DIAGRAM



## Low Phase Noise PLL Clock Multiplier

### PIN DESCRIPTIONS

Name	Number	Type	Description
CLK	1	O	Clock output from VCO. Equals the input frequency times multiplier.
REFEN	2	I	Reference clock enable. When Low, it turns off REFOUT.
VDD	3,4,5	P	3.3V Power Supply.
XIN	8	I	Crystal input to be connected to 10-30MHz fundamental parallel mode crystal ( $C_L=15\text{pF}$ ). On chip load capacitors: No external capacitor required.
XOUT	6	O	Crystal Connection.
OE	12	I	Output Enable. Tri-state CLK and REFOUT when low. Has internal pull-up.
REFOUT	13	O	Buffered crystal oscillator clock output. Controlled by REFEN.
S0	11	I	Multiplier Select Pin 0. Determines CLK output. Has internal pull-up.
S1	7	I	Multiplier Select Pin 1. Determines CLK output. Has internal pull-up.
S2	9	I	Multiplier Select Pin 1. Determines CLK output. Has internal pull-up.
S3	10	I	Multiplier Select Pin 3. Determines CLK output. Has internal pull-up.
GND	14,15,16	P	Ground.

## Low Phase Noise PLL Clock Multiplier

### ELECTRICAL SPECIFICATIONS

#### 1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	$V_{CC}$	-0.5	7	V
Input Voltage Range	$V_I$	-0.5	$V_{CC}+0.5$	V
Output Voltage Range	$V_O$	-0.5	$V_{CC}+0.5$	V
Soldering Temperature			260	°C
Storage Temperature	$T_S$	-65	150	°C
Ambient Operating Temperature		0	70	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

#### 2. AC Specification

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Frequency	Depends on selected multiplier	10		30	MHz
Output Frequency	At 3.3V			160	MHz
Output Rise Time	0.8V to 2.0V with no load			1.5	ns
Output Fall Time	2.0V to 0.8V with no load			1.5	ns
Duty Cycle	At VDD/2	45	50	55	%
Period jitter RMS	With capacitive decoupling between VDD and GND		6.4		ps
Accumulated jitter RMS	With capacitive decoupling between VDD and GND		9.4		ps
Phase Noise, relative to carrier, 155Mhz(x8)	100Hz offset, 3.3V		-103		dBc/Hz
Phase Noise, relative to carrier, 155Mhz(x8)	1kHz offset, 3.3V		-126		dBc/Hz
Phase Noise, relative to carrier, 155Mhz(x8)	10kHz offset, 3.3V		-133		dBc/Hz
Phase Noise, relative to carrier, 155Mhz(x8)	100kHz offset, 3.3V		-128		dBc/Hz

## Low Phase Noise PLL Clock Multiplier

### 3. DC Specification

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operating Voltage	VDD		3.135		3.465	V
Input High Voltage	V <sub>IH</sub>		2			V
Input Low Voltage	V <sub>IL</sub>				0.8	V
Input High Voltage	V <sub>IH</sub>	For XIN pin	(VDD/2) + 1	VDD/2		V
Input Low Voltage	V <sub>IL</sub>	For XIN pin		VDD/2	(VDD/2) – 1	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -25mA	2.4			V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 25mA			0.4	V
Output High Voltage At CMOS Level	V <sub>OH</sub>	I <sub>OH</sub> = -8mA	VDD-0.4			V
Operating Supply Current	I <sub>DD</sub>	No Load		35		mA
Short-circuit Current	I <sub>S</sub>			±120		mA
Input Capacitance	C <sub>IN</sub>	OE, Select Pins		5		pF

### 4. Crystal Specifications

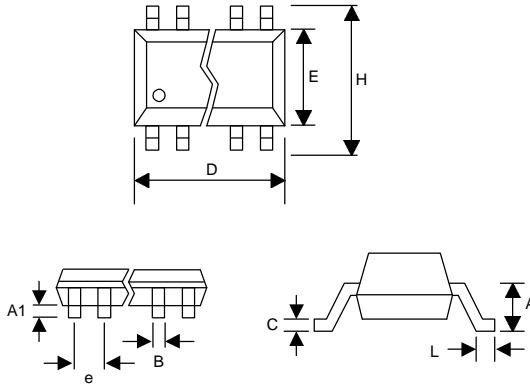
PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F <sub>XIN</sub>	Parallel Fundamental Mode	10		30	MHz
Crystal Loading Capacitance Rating	C <sub>L</sub> (xtal)			15		pF

## Low Phase Noise PLL Clock Multiplier

### PACKAGE INFORMATION

16 PIN Narrow SOIC, TSSOP ( mm )

	SOIC		TSSOP	
Symbol	Min.	Max.	Min.	Max.
A	1.35	1.75	-	1.20
A1	0.10	0.25	0.05	0.15
B	0.33	0.51	0.19	0.30
C	0.19	0.25	0.09	0.20
D	9.80	10.00	4.90	5.10
E	3.80	4.00	4.30	4.50
H	5.80	6.20	6.40 BSC	
L	0.40	1.27	0.45	0.75
e	1.27 BSC		0.65 BSC	



### ORDERING INFORMATION

**For part ordering, please contact our Sales Department:**

47745 Fremont Blvd., Fremont, CA 94538, USA  
Tel: (510) 492-0990 Fax: (510) 492-0991

#### PART NUMBER

The order number for this device is a combination of the following:  
Device number, Package type and Operating temperature range

**PLL601-03 X C**

PART NUMBER \_\_\_\_\_

TEMPERATURATURE  
C=COMMERCIAL  
M=MILITARY  
I=INDUSTRIAL

PACKAGE TYPE  
S=SOIC, O=TSSOP

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