Document Title

512Kx36 & 256Kx72 DLW(Double Late Write) RAM

Revision History

Rev. No.	History	Draft Date	Remark
0.0	1. Initial document.	November 2, 2000	Preliminary
0.1	1. Preliminary	March 30, 2001	Preliminary
0.2	1. Add scan order information	May 16, 2001	Preliminary
0.3	1. Part name change from K7N167285A to K7Z167285A	July 18, 2001	Preliminary
0.4	1. Device name change from Double Late Write SigmaRAM to Double Late Write RAM	Dec 17, 2001	Preliminary
0.5	1. Add x36 organization. 2. Add -20(200MHz) speed bin.	Feb. 06, 2002	Preliminary
0.6	1. Boundary scan exit order change	May. 14,2002	Preliminary

16Mb NtRAM(Flow Through / Pipelined) , Double Late Write RAM Ordering Information

Org.	Part Number	Mode	VDD	Speed FT ; Access Time(ns) Pipelined ; Cycle Time(MHz)	PKG	Temp
1Mx18	K7M161825A-Q(H/F)C(I)65/75/85	FlowThrough	3.3	6.5/7.5/8.5ns	Q : 100TQFP H : 119BGA F : 165FBGA	C (Commercial Temperature Range) I (Industrial Temperature Range)
	K7N161801A-Q(H/F)C(I)25/22/20/16/13	Pipelined	3.3	250/225/200/167/133MHz		
	K7N161845A-Q(H/F)C(I)25/22/20/16/13	Pipelined	2.5	250/225/200/167/133MHz		
512Kx32	K7M163225A-QC(I)65/75/85	FlowThrough	3.3	6.5/7.5/8.5ns		
	K7N163201A-QC(I)25/22/20/16/13	Pipelined	3.3	250/225/200/167/133MHz		
	K7N163245A-QC(I)25/22/20/16/13	Pipelined	2.5	250/225/200/167/133MHz		
512Kx36	K7M163625A-Q(H/F)C(I)65/75/85	FlowThrough	3.3	6.5/7.5/8.5ns		
	K7N163601A-Q(H/F)C(I)25/22/20/16/13	Pipelined	3.3	250/225/200/167/133MHz		
	K7N163645A-Q(H/F)C(I)25/22/20/16/13	Pipelined	2.5	250/225/200/167/133MHz		
	K7Z163685A-HC30/27/25/20	Pipelined (Sigma Type)	1.8	300/275/250/200MHz	H : 209BGA	
256Kx72	K7N167245A-HC25/22/20/16/13	Pipelined (Normal	2.5	250/225/200/167/133MHz	H : 209BGA	
	K7Z167285A-HC30/27/25/20	Pipelined (Sigma Type)	1.8	300/275/250/200MHz		

512Kx36 & 256Kx72-Bit DLW(Dobule Late Write) RAM

FEATURES

- Double Late Write mode , Pipelined Read mode.
- Compatible with Double Late Write Sigma RAM™ x36/x72.
- 1.8V+150/-100 mV Power Supply.
- 1.8V I/O supply.
- Byte Writable Function.
- Single READ/WRITE control pin.
- Self-Timed Write Cycle.
- Complement echo clock outputs
- Selectable impedance output buffer(ZQ)
- 2 User programmable chip enable inputs for easy depth expansion.(EP2, EP3)
- Supports linear burst mode only.
- Slow Down Function.
- IEEE 1149.1 JTAG Compatible Boundary Scan
- 209 bump, 14mm x 22mm, 1mm bump pitch BGA package
- 209BGA(11x19 Ball Grid Array Package).

FAST ACCESS TIMES

PARAMETER	Symbol	-30	-27	-25	-20	Unit
Cycle Time	t_{CYC}	3.3	3.6	4.0	5.0	ns
Clock Access Time	t_{CD}	1.8	2.0	2.1	2.3	ns

GENERAL DESCRIPTION

The K7Z163685A & K7Z167285A is 18,874,368-bits Synchronous Static SRAMs.

The Double Late Write RAM utilizes all the bandwidth in any combination of operating cycles.

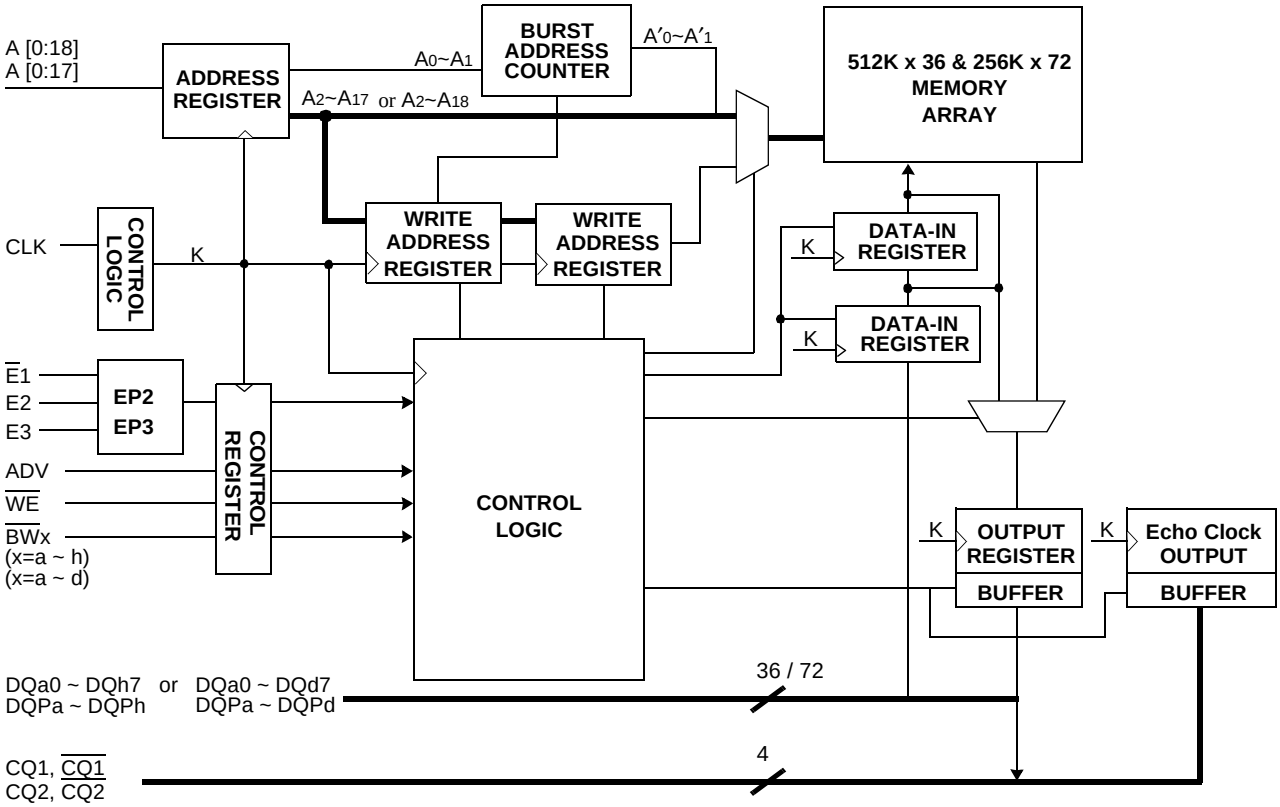
Address, data inputs, and all control signals except EP2, EP3, and $\overline{SD}$ are synchronized to input clock.

Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation and provides increased timing flexibility for incoming signals.

For read cycles,the SRAM output data is temporarily stored by an edge triggered output register and then released to the output buffers at the next rising edge of clock.

The K7Z163685A & K7Z167285A are implemented with SAMSUNG′s high performance CMOS technology and is available in 209BGA packages. Multiple power and ground pins minimize ground bounce.

LOGIC BLOCK DIAGRAM



209BGA PACKAGE PIN CONFIGURATIONS (TOP VIEW)

512Kx36 Common I/O-Top View

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC	A	E2	A	ADV	A	E3	A	DQb	DQb
B	NC	NC	$\overline{BW}$c	NC	A	$\overline{WE}$	A	$\overline{BW}$b	NC	DQb	DQb
C	NC	NC	NC	$\overline{BW}$d	NC(128M)	$\overline{E1}$	NC	NC	$\overline{BW}$a	DQb	DQb
D	NC	NC	V_{SS}	NC	NC	MCL	NC	NC	V_{SS}	DQb	DQb
E	NC	DQPc	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	NC	DQPb
F	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	ZQ	V_{SS}	V_{SS}	V_{SS}	NC	NC
G	DQc	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	EP2	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC
H	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	EP3	V_{SS}	V_{SS}	V_{SS}	NC	NC
J	DQc	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC
K	CQ2	$\overline{CQ2}$	CK	NC	V_{SS}	MCL	V_{SS}	NC	NC	$\overline{CQ1}$	CQ1
L	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
M	NC	NC	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
N	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	$\overline{SD}$	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
P	NC	NC	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
R	DQPd	NC	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQPa	NC
T	DQd	DQd	V_{SS}	NC	NC	MCL	NC	NC	V_{SS}	NC	NC
U	DQd	DQd	NC	A	NC(64M)	A	NC(32M)	A	NC	NC	NC
V	DQd	DQd	A	A	A	A1	A	A	A	NC	NC
W	DQd	DQd	TMS	TDI	A	A0	A	TDO	TCK	NC	NC

209BGA PACKAGE PIN CONFIGURATIONS (TOP VIEW)

256Kx72 Common I/O-Top View

	1	2	3	4	5	6	7	8	9	10	11
A	DQg	DQg	A	E2	A	ADV	A	E3	A	DQb	DQb
B	DQg	DQg	$\overline{BW}$c	$\overline{BW}$g	NC	$\overline{WE}$	A	$\overline{BW}$b	$\overline{BW}$f	DQb	DQb
C	DQg	DQg	$\overline{BW}$h	$\overline{BW}$d	NC(128M)	$\overline{E1}$	NC	$\overline{BW}$e	$\overline{BW}$a	DQb	DQb
D	DQg	DQg	V_{SS}	NC	NC	MCL	NC	NC	V_{SS}	DQb	DQb
E	DQPg	DQPc	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQPf	DQPb
F	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	ZQ	V_{SS}	V_{SS}	V_{SS}	DQf	DQf
G	DQc	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	EP2	V_{DD}	V_{DDQ}	V_{DDQ}	DQf	DQf
H	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	EP3	V_{SS}	V_{SS}	V_{SS}	DQf	DQf
J	DQc	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	DQf	DQf
K	CQ2	$\overline{CQ2}$	CK	NC	V_{SS}	MCL	V_{SS}	NC	NC	$\overline{CQ1}$	CQ1
L	DQh	DQh	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
M	DQh	DQh	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
N	DQh	DQh	V_{DDQ}	V_{DDQ}	V_{DD}	$\overline{SD}$	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
P	DQh	DQh	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
R	DQPd	DQPh	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQPa	DQPe
T	DQd	DQd	V_{SS}	NC	NC	MCL	NC	NC	V_{SS}	DQe	DQe
U	DQd	DQd	NC	A	NC(64M)	A	NC(32M)	A	NC	DQe	DQe
V	DQd	DQd	A	A	A	A1	A	A	A	DQe	DQe
W	DQd	DQd	TMS	TDI	A	A0	A	TDO	TCK	DQe	DQe

Pin Description Table

Pin Name	Description	Type	Comments
A	Address	Input	-
ADV	Advance	Input	Active High
$\overline{BW}$x(x=a~h or a~d)	Byte Write Enable	Input	Active Low
CK	Clock	Input	Active High
DQ	Data I/O	Input/Output	-
CQ	Echo Clock Outputs	Output	Active High
$\overline{CQ}$	Echo Clock Outputs	Output	Active Low
$\overline{E1}$	Chip Enable	Input	Active Low
E2 & E3	Chip Enable	Input	Programmable Active High or Low
EP2 & EP3	Chip Enable Program Pin	Input	-
$\overline{SD}$	Slow Down Input	Input	Active Low
TCK	Test Clock	Input	Active High
TDI	Test Data In	Input	-
TDO	Test Data Out	Output	-
TMS	Test Mode Select	Input	-
MCH	Must Connect High	Input	Active High
MCL	Must Connect Low	Input	Active Low
NC	No Connect	-	Not connected to die
$\overline{WE}$	Write	Input	Active Low
V_{DD}	Core Power Supply	Input	1.8V
V_{DDQ}	Output Driver Power Supply	Input	1.8V
V_{SS}	Ground	Input	-
ZQ	Output Impedance Control	Input	Low = Low Impedance(High Drive) High = High Impedance(Low Drive)

FUNCTION DESCRIPTION

The K7Z163685A & K7Z167285A is Double Late Write RAM designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa.
Because a Double Late Write RAM is a synchronous device, address, data Inputs, and read/write control inputs are captured on the rising edge of the input clock. EP2 , EP3 and $\overline{SD}$ are asynchronous control input.

Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register, all three chip enables($\overline{E1}$, E2, E3) are active, the write enable input signals $\overline{WE}$ are driven high, and ADV driven low.The internal array is read between the first rising edge and the second rising edge of the clock and the data is latched in the output register. At the second clock edge the data is driven out of the SRAM.

Write operation occurs when $\overline{WE}$ is driven low at the rising edge of the clock. $\overline{BW}$x[h:a] can be used for byte write operation.
The Double Late Write RAM uses a double-late write cycle to utilize 100% of the bandwidth.
At the first rising edge of the clock, $\overline{WE}$ and address are registered, and the data associated with that address is required two cycle later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst seguence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

Double Late Write RAM supports linear burst sequence only.

BURST SEQUENCE TABLE (Linear Burst Order)

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Slow Down Function

$\overline{SD}$ is helpful to prevent to bus contention in read operation after write operation , especially high frequency application.
When $\overline{SD}$ is Low, the SRAM is operated in a slow down mode. In a slow down mode, the enable/disable timings of output data become slower , which are defined as tKHQV,tKHQZ,tKHQX,tKHQX1/tKHCH and tKLCL.
The valid data window in slow down mode is same with normal operation mode , so it will be helpful in read operation after write operation
When $\overline{SD}$ is High , the SRAM returns to normal operation node.
The state of $\overline{SD}$ must be fixed before operation , and it can not be changed during operation.

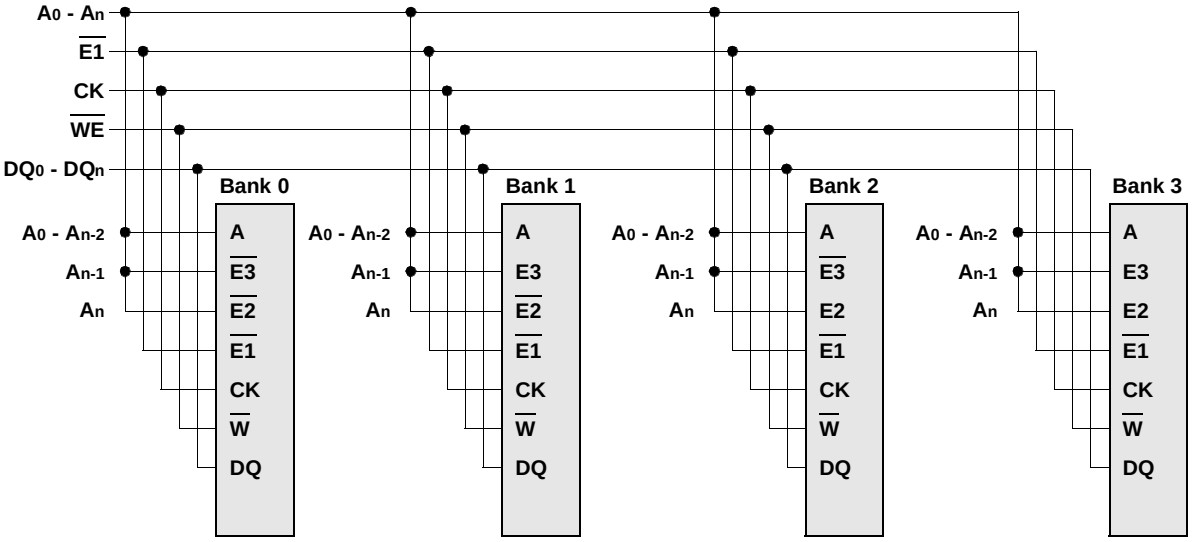
Programmable Enables

Double Late Write RAM features two user programmable chip enable inputs, E2 and E3. The sense of the inputs, whether they function as active low or active high inputs, is determined by the state of the programming inputs, EP2 and EP3. For example, if EP2 is held at V_{DD}, E2 functions as an active high enable. If EP2 is held to VSS, E2 functions as an active low chip enable input.

Programmability of E2 and E3 allows four banks of depth expansion to be accomplished with no additional logic. By programming the enable inputs of four Double Late Write RAMs in binary sequence(00, 01, 10, 11)and driving the enable inputs with two address inputs. Four Double Late Write RAM can be made to look like one larger RAM to the system.

Deselection of the RAM via $\overline{E1}$ does not deactive the Echo Clocks.

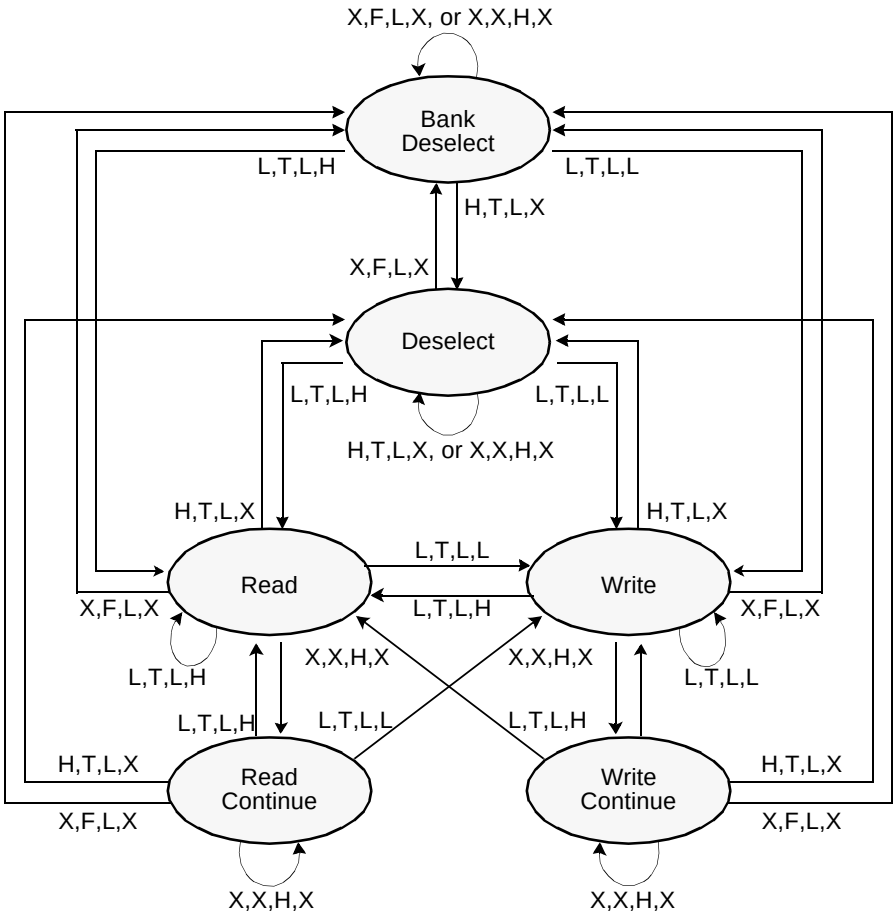
Example Four Bank Depth Expansion Schematic



Bank Enable Truth Table

	EP2	EP3	E2	E3
Bank 0	V_{SS}	V_{SS}	Active Low	Active Low
Bank 1	V_{SS}	V_{DD}	Active Low	Active High
Bank 2	V_{DD}	V_{SS}	Active High	Active Low
Bank 3	V_{DD}	V_{DD}	Active High	Active High

STATE DIAGRAM FOR Double Late Write RAM



Notes:
1. The notation "X,X,X,X" controlling the state transitions above indicate the states of inputs $\overline{E1}$,E,ADV, and $\overline{WE}$ respectively.
2. If (E2=EP2 and E3=EP3) then E="T" else E="F".
3. "H"=input "high"; "L"=input"low"; "X"=input"dont care"; "T"=input "true"; "F"=input "false".

TRUTH TABLES

Previous Cycle	Input Type	$\overline{E1}$ (tn)	E (tn)	ADV (tn)	$\overline{WE}$ (tn)	$\overline{BWx}$ (tn)	Current Operation	Address	DQ/CQ (tn)	DQ/CQ (tn+1)	Notes
N/A	D	H	T	L	X	X	Deselect Cycle	None	*	Hi-Z/CQ	4
Deselect	C	X	X	H	X	X	Deselect Cycle, Continue	Next	Hi-Z/CQ	Hi-Z/CQ	4
N/A	D	X	F	L	X	X	Bank Deselect Cycle	None	*	Hi-Z	4, 5
Bank Deselect	C	X	X	H	X	X	Bank Deselect Cycle, Continue	Next	Hi-Z	Hi-Z	4 , 5
N/A	R	L	T	L	H	X	Read Cycle, Begin Burst	External	*	Q/CQ	2
Read	C	X	X	H	X	X	Read Cycle, Continue Burst	Next	Q/CQ	Q/CQ	
N/A	W	L	T	L	L	X	Write Cycle, Begin Burst	External	*	D/CQ	2, 3
N/A	W	L	T	L	L	F	Non-Write Cycle, Begin Burst	External	*	*	2, 3
Write	C	X	X	H	X	T	Write Cycle, Continue Burst	Next	D/CQ	D/CQ	3
Write	C	X	X	H	X	F	Non-Write Cycle, Continue Burst	Next	*	D/CQ	3, 4, 5

Note:
1. X=Dont Care, H=High, L=Low.
2. E=T(True) if E2=active and E3=active; E=F(False) if E2=inactive or E3=inactive.
3. " * " indicates that the DQ input requirement / output state and CQ output state are determined by the previous operation.
4. $\overline{BW}$x= F(False) if all Byte Write Enable pins are high. $\overline{BW}$x=T(True) if any one Byte Write Enable pin is low.
5. DQs are tri-state in response to Bank Deselect, Deselect, and Write commands.
6. Deassertion of $\overline{E1}$ does not deactive the echo clock outputs(CQ1,$\overline{CQ1}$, CQ2, $\overline{CQ2}$).

   Echo clock outputs are tri-stated in response to Bank Deselect Commands only.

WRITE TRUTH TABLE(x36)

$\overline{WE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$	OPERATION
H	X	X	X	X	READ
L	L	H	H	H	WRITE BYTE a
L	H	L	H	H	WRITE BYTE b
L	H	H	L	H	WRITE BYTE c
L	H	H	H	L	WRITE BYTE d
L	L	L	L	L	WRITE ALL BYTEs
L	H	H	H	H	WRITE ABORT/NOP

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

WRITE TRUTH TABLE(x72)

$\overline{WE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$	$\overline{BWe}$	$\overline{BWf}$	$\overline{BWg}$	$\overline{BWh}$	OPERATION
H	X	X	X	X	X	X	X	X	READ
L	L	H	H	H	H	H	H	H	WRITE BYTE a
L	H	L	H	H	H	H	H	H	WRITE BYTE b
L	H	H	L	H	H	H	H	H	WRITE BYTE c
L	H	H	H	L	H	H	H	H	WRITE BYTE d
L	H	H	H	H	L	H	H	H	WRITE BYTE e
L	H	H	H	H	H	L	H	H	WRITE BYTE f
L	H	H	H	H	H	H	L	H	WRITE BYTE g
L	H	H	H	H	H	H	H	L	WRITE BYTE h
L	L	L	L	L	L	L	L	L	WRITE ALL BYTEs
L	H	H	H	H	H	H	H	H	WRITE ABORT/NOP

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.3 to 2.5	V
Voltage on Any Other Pin Relative to V_{SS}	V_{IN}	-0.3 to VDD+0.3	V
Power Dissipation	P_D	1.6	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_{OPR}	0 to 70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	°C

***Note** : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS($0°C \le T_A \le 70°C$)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V_{DD}	1.7	1.8	1.95	V
	V_{DDQ}	1.7	1.8	1.95	V
Ground	V_{SS}	0	0	0	V

***Note** : V_{DD} and V_{DDQ} must be supplied with identical voltage levels.

Selectable Impedance Output Driver DC ELECTRICAL CHARACTERISTICS

The K7Z167285A is supplied with selectable (high or low) impedance output buffers.

ZQ=VDDQ

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Low Drive Output Low Voltage	V_{OLL}	I_{OL}=4.0mA	-	0.4	V
Low Drive Output High Voltage	V_{OHL}	I_{OH}=-4.0mA	V_{DDQ} - 0.4	-	V

ZQ=0V

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
High Drive Output Low Voltage	V_{OLH}	I_{OL}= 8.0mA	-	0.4	V
High Drive Output High Voltage	V_{OHH}	I_{OH}=-8.0mA	V_{DDQ} - 0.4	-	V

***Note** : The ZQ level supplied with selectable impedance allows selection between high drive strength (ZQ=Low) and low drive strength (ZQ=High).

CAPACITANCE*(T_A=25°C, f=1MHz)

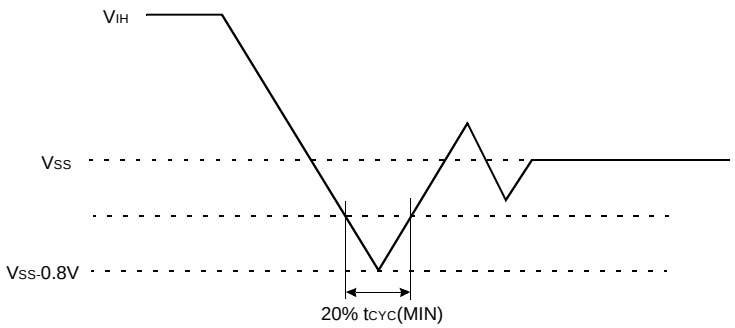
PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

***Note** : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS(V_{DD}=1.8V + 150/-100mV, T_A=0°C to +70°C)

PARAMETER	SYMBOL	TEST CONDITIONS			MIN	MAX	UNIT	NOTES
Input Leakage Current	I_{IL}	V_{DD}=Max ; V_{IN}=V_{SS} to V_{DD}			-2	+2	µA	
Output Leakage Current	I_{OL}	Output Disabled,			-2	+2	µA	
Operating Current	I_{CC}	V_{DD}=Max , I_{OUT}=0mA Cycle Time ≥ t_{CYC} Min	-30	x72	-	720	mA	1,2
				x36	-	TBD		
			-27	x72	-	670		
				x36		TBD		
			-25	x72		620		
				x36		TBD		
			-20	x72		540		
				x36		TBD		
Standby Current	I_{SB1}	E2 or E3 False, I_{OUT}=0mA , f=Max All Inputs≤V_{IL} or ≥V_{IH}			-	120	mA	
	I_{SB2}	$\overline{E1}$ ≥V_{IH}, I_{OUT}=0mA, f=Max, All Inputs≤V_{IL} or ≥V_{IH}			-	150	mA	
	I_{SB3}	Device deselected, I_{OUT}=0mA, f=0, All Inputs=fixed (V_{DD}-0.2V or 0.2V)			-	50	mA	
Input Low Voltage	V_{IL}				-0.3	0.3*V_{DDQ}	V	3
Input Low Voltage for EP2,EP3,$\overline{SD}$	V_{IL1}				-0.3	0.3	V	
Input High Voltage	V_{IH}				0.7*V_{DDQ}	V_{DD}+0.3	V	3
Input High Voltage for EP2,EP3,$\overline{SD}$	V_{IH1}				V_{DD} - 0.3	V_{DD}+0.3	V	

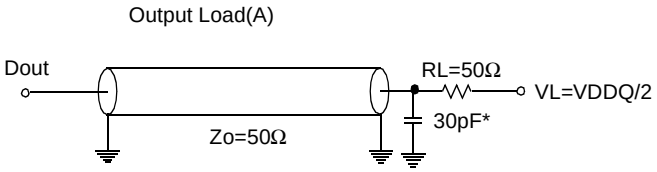
Notes : 1. Reference AC Operating Conditions and Characteristics for input and timing.
2. Data states are all zero.
3. In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.3V
4. The EP2, EP3 pins must not be changed during operation.



TEST CONDITIONS(T_A=0 to 70°C, V_{DD}=1.8V + 150/-100mV, unless otherwise specified)

PARAMETER	VALUE
Input Pulse Level	0 to 1.8V
Input Rise and Fall Time(Measured at 20% to 80%)	2.0V/ns
Input and Output Timing Reference Levels	0.9V
Output Load	See Fig. 1

AC Test Load Diagram



* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS when /SD=VDD (V_{DD}=1.8V + 150/-100mV, T_A=0 to 70°C)

PARAMETER	SYMBOL	-30		-27		-25		-20		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	t_{KHKH}	3.3	-	3.6	-	4.0	-	5.0	-	ns
Clock High to Output Valid	t_{KHQV}	-	1.8	-	2.0	-	2.1	-	2.3	ns
Clock High to Output High-Z	t_{KHQZ}	0.5	1.8	0.5	2.0	0.5	2.1	0.5	2.3	ns
Output Hold from Clock High	t_{KHQX}	0.5	-	0.5	-	0.5	-	0.5	-	ns
Clock High to Output Low-Z	t_{KHQX1}	0.5	-	0.5	-	0.5	-	0.5	-	ns
Clock High to CQ High	t_{KHCH}	0.5	1.9	0.5	2.0	0.5	2.3	0.5	2.4	ns
Clock Low to CQ Low	t_{KLCL}	0.5	1.9	0.5	2.0	0.5	2.3	0.5	2.4	ns
Output Hold from CQ High	t_{CHQX}	-0.4	-	-0.4	-	-0.5	-	-0.6	-	ns
CQ High to Output Low-Z	t_{CHQX1}	-0.4	-	-0.4	-	-0.5	-	-0.6	-	ns
CQ High to Output Valid	t_{CHQV}	-	0.4	-	0.4	-	0.5	-	0.6	ns
Clock High to CQ Low-Z	t_{KHCX1}	0.5	-	0.5	-	0.5	-	0.5	-	ns
Clock High to CQ High-Z	t_{KHCZ}	0.5	1.7	0.5	1.9	0.5	2.0	0.5	2.1	ns
Clock High Pulse Width	t_{KHKL}	1.3	-	1.4	-	1.5	-	1.6	-	ns
Clock Low Pulse Width	t_{KLKH}	1.3	-	1.4	-	1.5	-	1.6	-	ns
Address Setup to Clock High	t_{AVKH}	0.7	-	0.7	-	0.8	-	0.9	-	ns
Chip Enable Setup to Clock High	t_{EVKH}	0.7	-	0.7	-	0.8	-	0.9	-	ns
Write Setup to Clock High($\overline{WE}$, $\overline{BW}$x)	t_{WVKH}	0.7	-	0.7	-	0.8	-	0.9	-	ns
Data Setup to Clock High	t_{DVKH}	0.7	-	0.7	-	0.8	-	0.9	-	ns
Address Advance Setup to Clock High	t_{advVKH}	0.7	-	0.7	-	0.8	-	0.9	-	ns
Address Hold from Clock High	t_{KHAX}	0.4	-	0.4	-	0.5	-	0.6	-	ns
Chip Enable Hold from Clock High	t_{KHEX}	0.4	-	0.4	-	0.5	-	0.6	-	ns
Write Hold from Clock High($\overline{WE}$, $\overline{BW}$x)	t_{KHWX}	0.4	-	0.4	-	0.5	-	0.6	-	ns
Data Hold from Clock High	t_{KHDX}	0.4	-	0.4	-	0.5	-	0.6	-	ns
Address Advance Hold from Clock High	t_{KHadvX}	0.4		0.4		0.5	-	0.6	-	ns

Notes : 1. All address inputs must meet the specified setup and hold times for all rising clock(CLK) edges when ADV is sampled low and $\overline{E1}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Chip selects must be valid at each rising edge of CLK(when ADV is Low) to remain enabled.
3. A write cycle is defined by $\overline{WE}$ low having been registered into the device at ADV Low, A Read cycle is defined by $\overline{WE}$ High with ADV Low, Both cases must meet setup and hold times.
4. To avoid bus contention, At a given voltage and temperature t_{KHQX1} is more than t_{KHQZ}.
The specs as shown do not imply bus contention because t_{KHQX1} is a Min. parameter that is worst case at totally different test conditions (0°C,1.95V) than t_{KHQZ}, which is a Max. parameter(worst case at 70°C,1.7V)
It is not possible for two SRAMs on the same board to be at such different voltage and temperature.

AC TIMING CHARACTERISTICS when /SD=VSS (V_{DD}=1.8V + 150/-100mV, T_A=0 to 70°C)

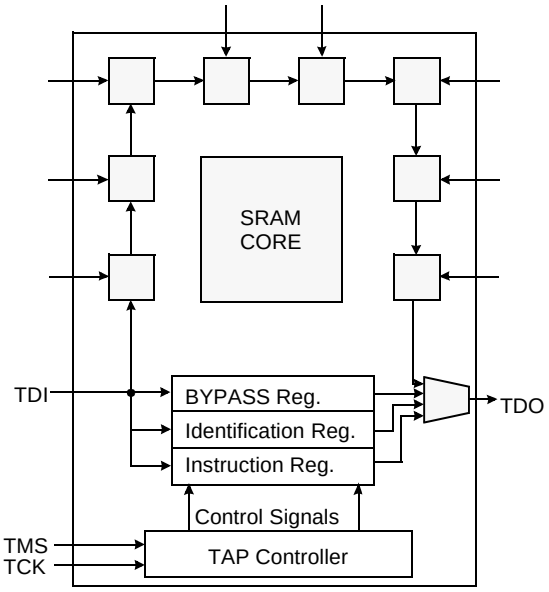
PARAMETER	SYMBOL	-30		-27		-25		-20		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	t_{KHKH}	3.3	-	3.6	-	4.0	-	5.0	-	ns
Clock High to Output Valid	t_{KHQV}	-	2.7	-	2.9	-	3.0	-	3.2	ns
Clock High to Output High-Z	t_{KHQZ}	1.4	2.7	1.4	2.9	1.4	3.0	1.4	3.2	ns
Output Hold from Clock High	t_{KHQX}	1.4	-	1.4	-	1.4	-	1.4	-	ns
Clock High to Output Low-Z	t_{KHQX1}	1.4	-	1.4	-	1.4	-	1.4	-	ns
Clock High to CQ High	t_{KHCH}	1.4	2.8	1.4	2.9	1.4	3.2	1.4	3.3	ns
Clock Low to CQ Low	t_{KLCL}	1.4	2.8	1.4	2.9	1.4	3.2	1.4	3.3	ns
Output Hold from CQ High	t_{CHQX}	-0.4	-	-0.4	-	-0.5	-	-0.6	-	ns
CQ High to Output Low-Z	t_{CHQX1}	-0.4	-	-0.4	-	-0.5	-	-0.6	-	ns
CQ High to Output Valid	t_{CHQV}	-	0.4	-	0.4	-	0.5	-	0.6	ns
Clock High to CQ Low-Z	t_{KHCX1}	1.4	-	1.4	-	1.4	-	1.4	-	ns
Clock High to CQ High-Z	t_{KHCZ}	1.4	2.6	1.4	2.8	1.4	2.9	1.4	3.0	ns
Clock High Pulse Width	t_{KHKL}	1.3	-	1.4	-	1.5	-	1.6	-	ns
Clock Low Pulse Width	t_{KLKH}	1.3	-	1.4	-	1.5	-	1.6	-	ns
Address Setup to Clock High	t_{AVKH}	0.7	-	0.7	-	0.8	-	0.9	-	ns
Chip Enable Setup to Clock High	t_{EVKH}	0.7	-	0.7	-	0.8	-	0.9	-	ns
Write Setup to Clock High($\overline{W}$, $\overline{BW}$x)	t_{WVKH}	0.7	-	0.7	-	0.8	-	0.9	-	ns
Data Setup to Clock High	t_{DVKH}	0.7	-	0.7	-	0.8	-	0.9	-	ns
Address Advance Setup to Clock High	t_{advVKH}	0.7	-	0.7	-	0.8	-	0.9	-	ns
Address Hold from Clock High	t_{KHAX}	0.4	-	0.4	-	0.5	-	0.6	-	ns
Chip Enable Hold from Clock High	t_{KHEX}	0.4	-	0.4	-	0.5	-	0.6	-	ns
Write Hold from Clock High($\overline{W}$, $\overline{BW}$x)	t_{KHWX}	0.4	-	0.4	-	0.5	-	0.6	-	ns
Data Hold from Clock High	t_{KHDX}	0.4	-	0.4	-	0.5	-	0.6	-	ns
Address Advance Hold from Clock High	t_{KHadvX}	0.4		0.4		0.5	-	0.6	-	ns

Notes : 1. All address inputs must meet the specified setup and hold times for all rising clock(CLK) edges when ADV is sampled low and $\overline{E1}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Chip selects must be valid at each rising edge of CLK(when ADV is Low) to remain enabled.
3. A write cycle is defined by W low having been registered into the device at ADV Low, A Read cycle is defined by $\overline{W}$ High with ADV Low, Both cases must meet setup and hold times.
4. To avoid bus contention, At a given voltage and temperature t_{KHQX1} is more than t_{KHQZ}.
The specs as shown do not imply bus contention because t_{KHQX1} is a Min. parameter that is worst case at totally different test conditions (0°C,1.95V) than t_{KHQZ}, which is a Max. parameter(worst case at 70°C,1.7V)
It is not possible for two SRAMs on the same board to be at such different voltage and temperature.

IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Test Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to V_{SS} to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a resistor. TDO should be left unconnected.

JTAG Block Diagram



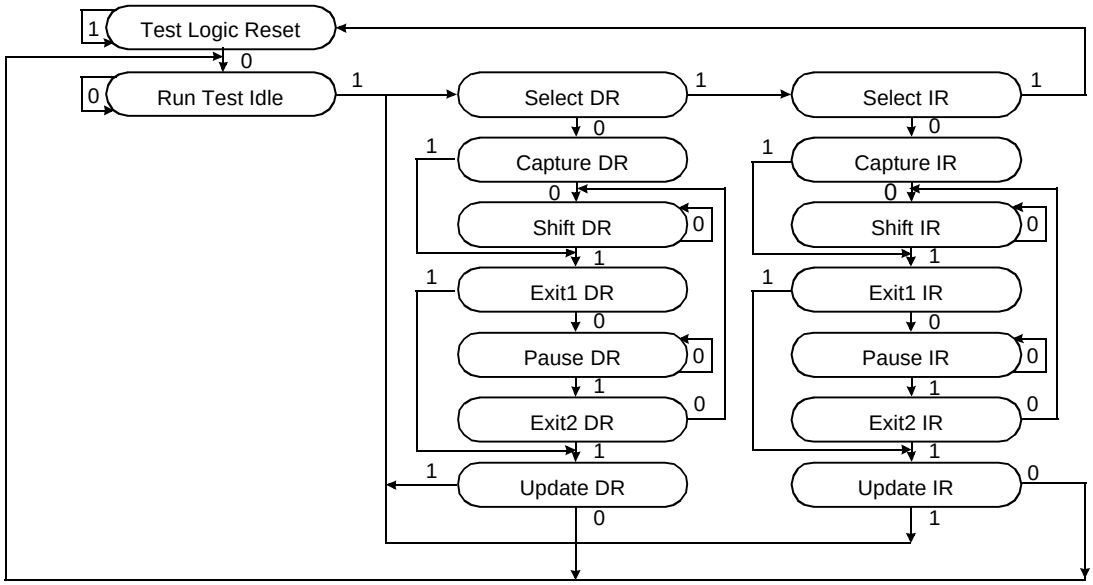
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	EXTEST	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	3
0	1	0	SAMPLE-Z	Boundary Scan Register	2
0	1	1	BYPASS	Bypass Register	4
1	0	0	SAMPLE	Boundary Scan Register	5
1	0	1	RESERVED	Do Not Use	6
1	1	0	BYPASS	Bypass Register	4
1	1	1	BYPASS	Bypass Register	4

NOTE :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs. This instruction is not IEEE 1149.1 compliant.
2. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
3. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
4. Bypass register is initiated to V_{SS} when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
5. SAMPLE instruction dose not places DQs in Hi-Z.
6. This instruction is reserved for future use.

TAP Controller State Diagram



SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
512Kx36	3 bits	1 bits	32 bits	120 bits
256Kx72	3 bits	1 bits	32 bits	120 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
512Kx36	0000	00111 00100	XXXXXX	00001001110	1
256Kx72	0000	00110 00101	XXXXXX	00001001110	1

BOUNDARY SCAN EXIT ORDER(x36/x72)

Bit	x36	x72		Bit #	x36	x72
1	6W	6W		36	10C	11H
2	6V	6V		37	NC	10H
3	6U	6U		38	11B	10G
4	7V	7V		39	NC	11G
5	7U	7U		40	10A	11F
6	7W	7W		41	NC	10F
7	8U	8U		42	NC	10E
8	8V	8V		43	11E	11E
9	9V	9V		44	NC	11D
10	10R	10W		45	10D	10D
11	NC	11W		46	NC	10C
12	10P	11V		47	11C	11C
13	NC	10V		48	NC	11B
14	11N	10U		49	10B	10B
15	NC	11U		50	NC	10A
16	10M	11T		51	11A	11A
17	NC	10T		52	9C	9C
18	11L	11R		53	9B	9B
19	NC	10R		54	9A	9A
20	NC	10P		55	8C	8C
21	11P	11P		56	8B	8B
22	NC	11N		57	8A	8A
23	10N	10N		58	7B	7B
24	NC	10M		59	7A	7A
25	11M	11M		60	6H	6H
26	NC	11L		61	6G	6G
27	10L	10L		62	6D	6D
28	11K	11K		63	6C	6C
29	6M	6M		64	6B	6B
30	6L	6L		65	6A	6A
31	6J	6J		66	5C	5C
32	6F	6F		67	5A	5A
33	10K	10K		68	4C	4C
34	11D	10J		69	4B	4B
35	NC	11J		70	5B	5B

Bit	X36	X72		Bit	x36	x36
71	4A	4A		106	1R	1R
72	3C	3C		107	NC	1T
73	3B	3B		108	2T	2T
74	3A	3A		109	NC	2U
75	2E	2A		110	1U	1U
76	NC	1A		111	NC	1V
77	2F	1B		112	2V	2V
78	NC	2B		113	NC	2W
79	1G	2C		114	1W	1W
80	NC	1C		115	3V	3V
81	2H	1D		116	4V	4V
82	NC	2D		117	4U	4U
83	1J	1E		118	5U	5U
84	NC	2E		119	5V	5V
85	NC	2F		120	5W	5W
86	1F	1F				
87	NC	1G				
88	2G	2G				
89	NC	2H				
90	1H	1H				
91	NC	1J				
92	2J	2J				
93	1K	1K				
94	3K	3K				
95	4K	4K				
96	2K	2K				
97	1T	2L				
98	NC	1L				
99	2U	1M				
100	NC	2M				
101	1V	2N				
102	NC	1N				
103	2W	1P				
104	NC	2P				
105	NC	2R				

NOTE, NC ; Don't Care

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V_{DD}	1.7	1.8	1.95	V	
Input High Level	V_{IH}	1.05	-	V_{DD}+0.3	V	1
Input Low Level	V_{IL}	-0.3	-	0.7	V	
Output High Voltage(I_{OH}=-2mA)	V_{OH}	1.5	-	V_{DD}	V	
Output Low Voltage(I_{OL}=2mA)	V_{OL}	V_{SS}	-	0.45	V	

***Note** : 1. In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.3V

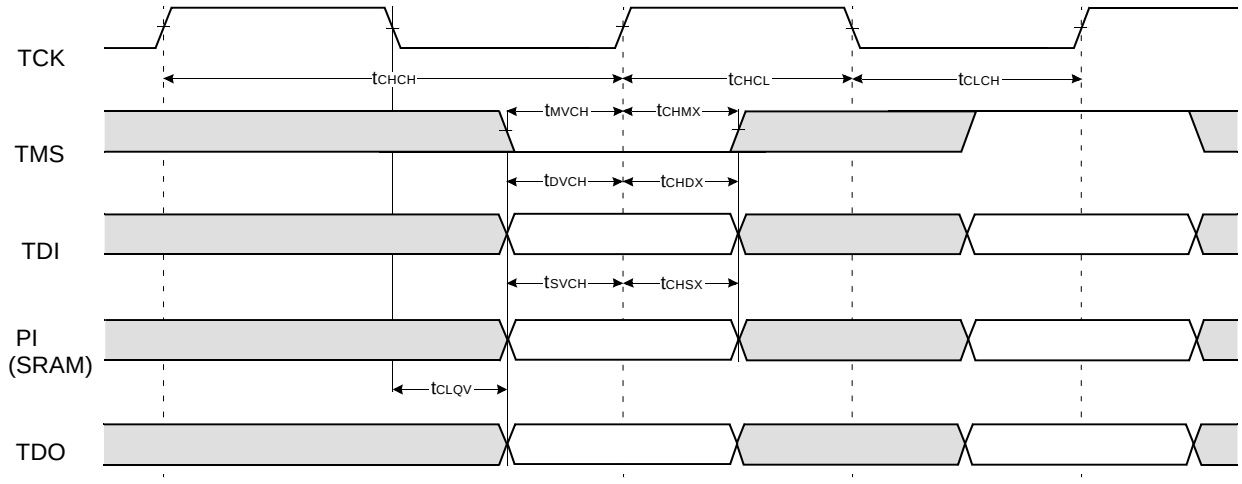
JTAG AC TEST CONDITIONS

Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V_{IH}/V_{IL}	1.8/0.0	V	
Input Rise/Fall Time	TR/TF	1.0/1.0	ns	
Input and Output Timing Reference Level		0.9	V	

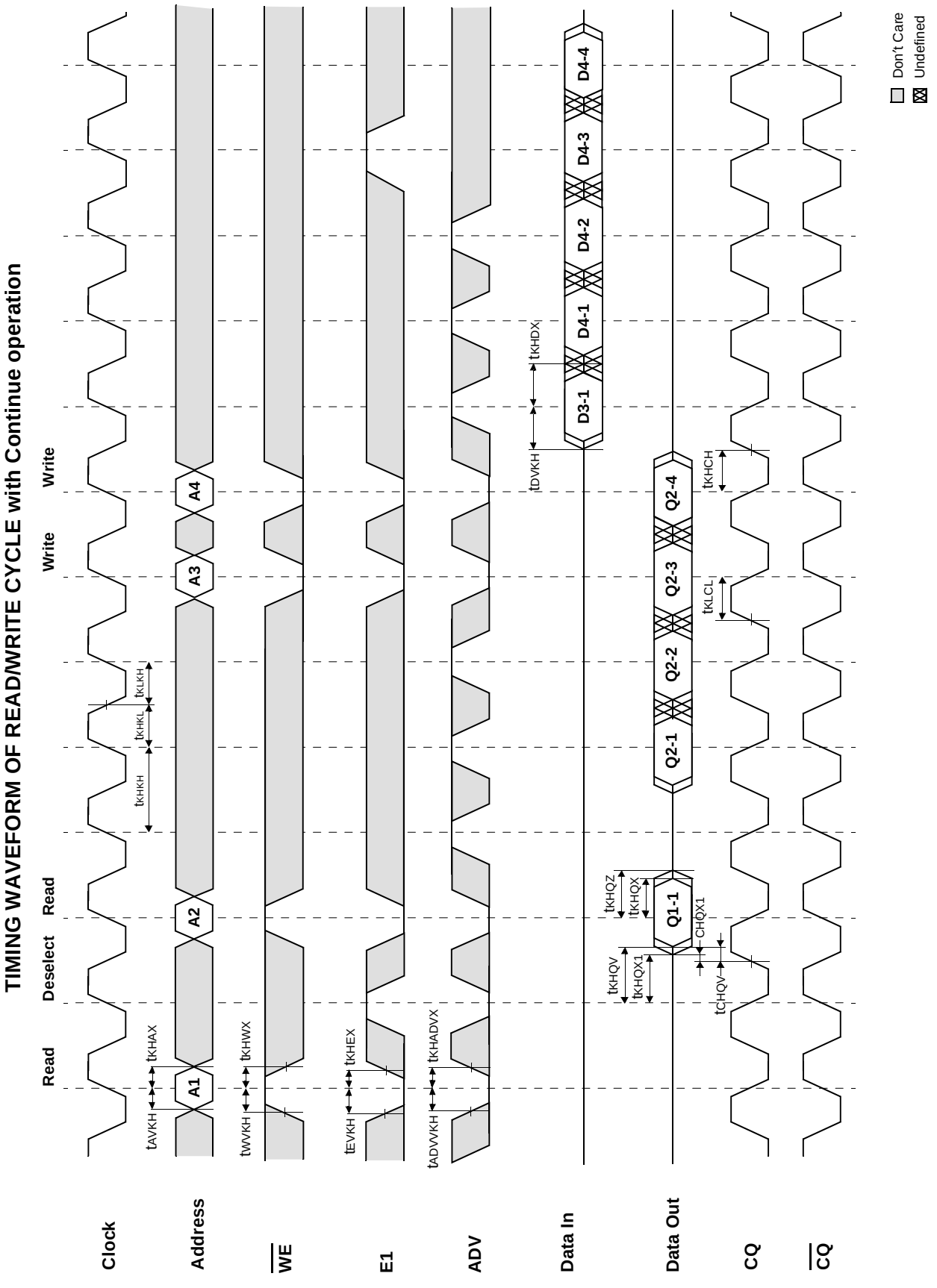
JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t_{CHCH}	20	-	ns	
TCK High Pulse Width	t_{CHCL}	10	-	ns	
TCK Low Pulse Width	t_{CLCH}	10	-	ns	
TMS Input Setup Time	t_{MVCH}	5	-	ns	
TMS Input Hold Time	t_{CHMX}	5	-	ns	
TDI Input Setup Time	t_{DVCH}	5	-	ns	
TDI Input Hold Time	t_{CHDX}	5	-	ns	
SRAM Input Setup Time	t_{SVCH}	5	-	ns	
SRAM Input Hold Time	t_{CHSX}	5	-	ns	
Clock Low to Output Valid	t_{CLQV}	0	10	ns	

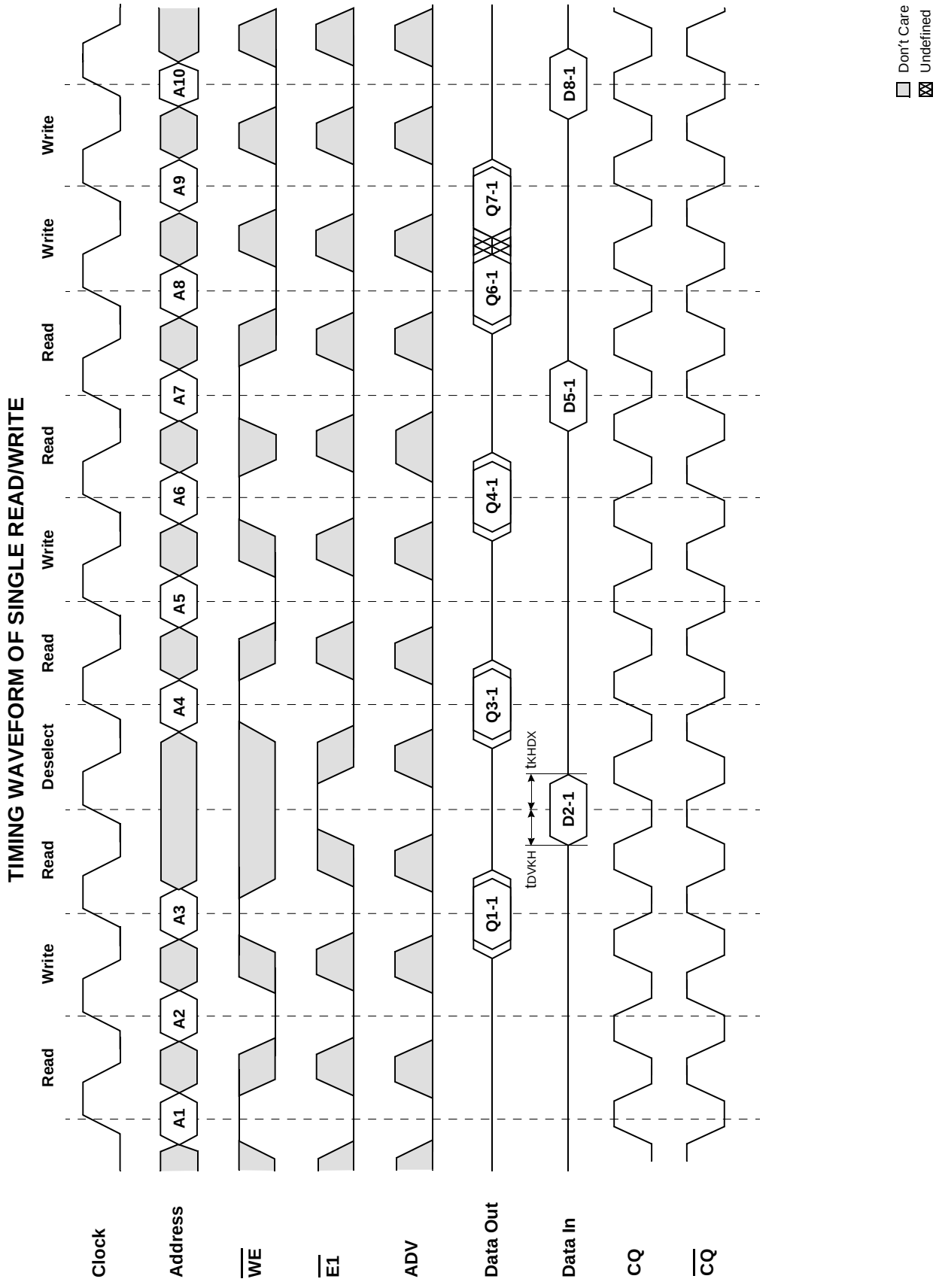
JTAG TIMING DIAGRAM



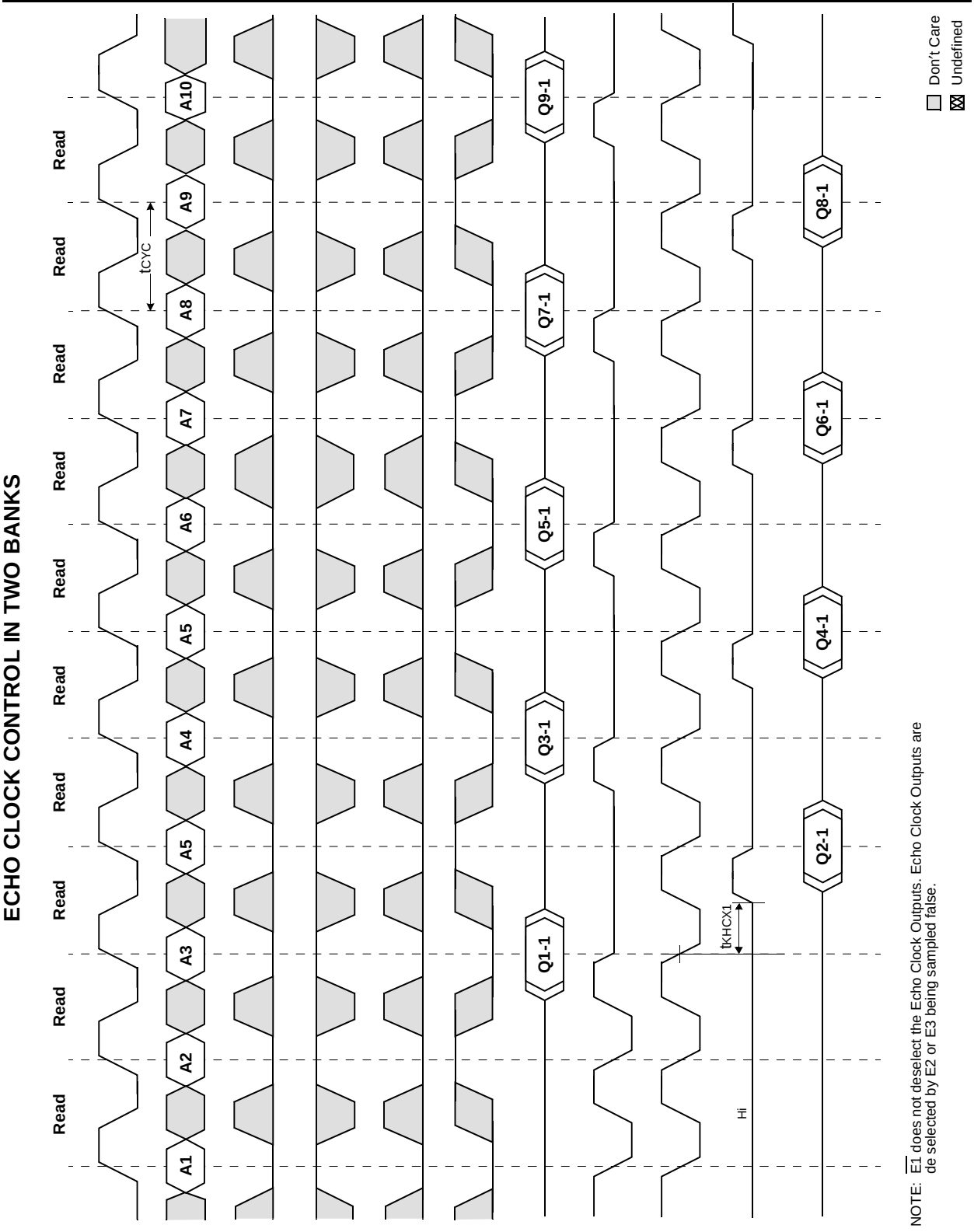
TIMING WAVEFORM OF READ/WRITE CYCLE with Continue operation



TIMING WAVEFORM OF SINGLE READ/WRITE

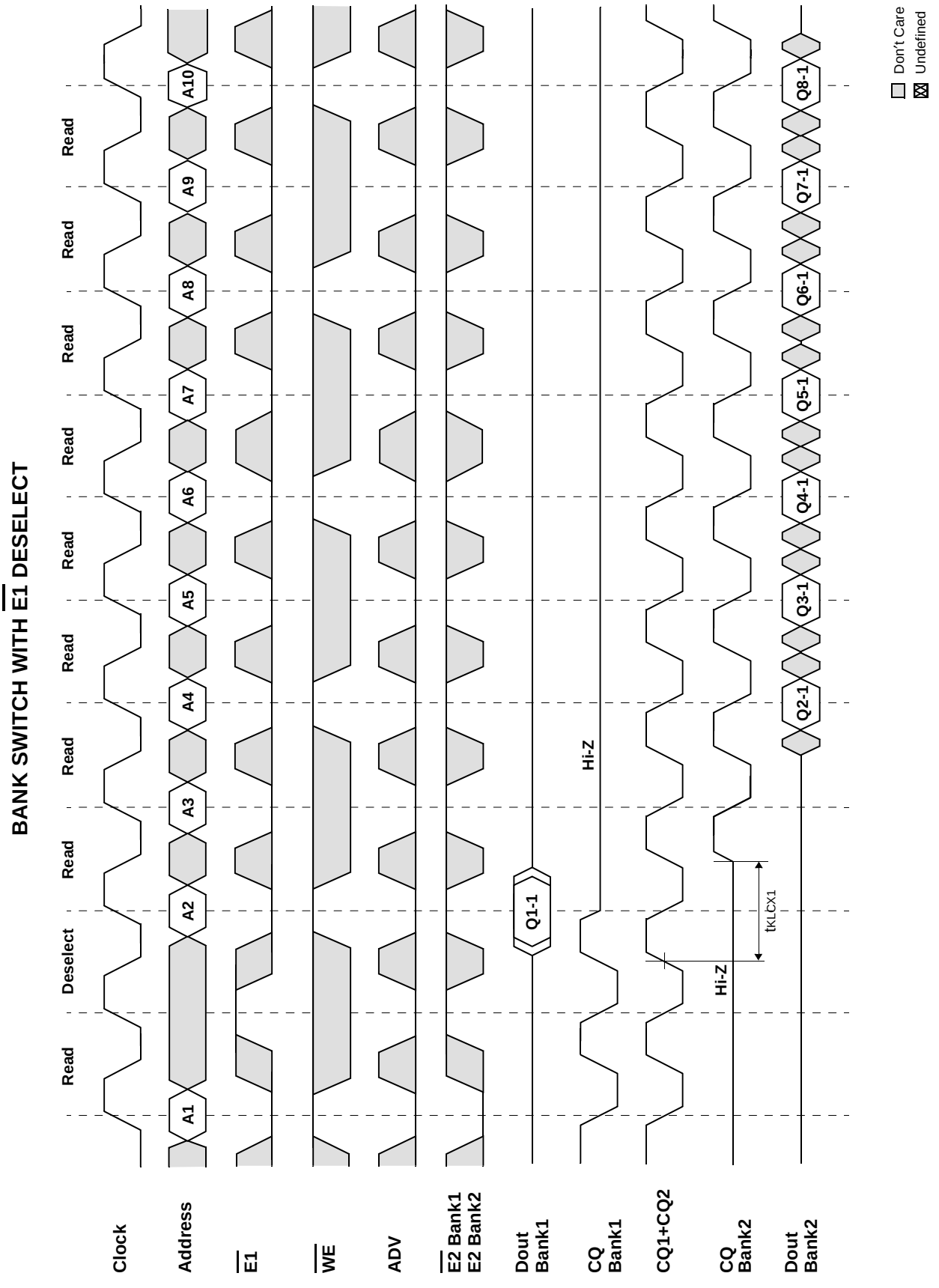


ECHO CLOCK CONTROL IN TWO BANKS



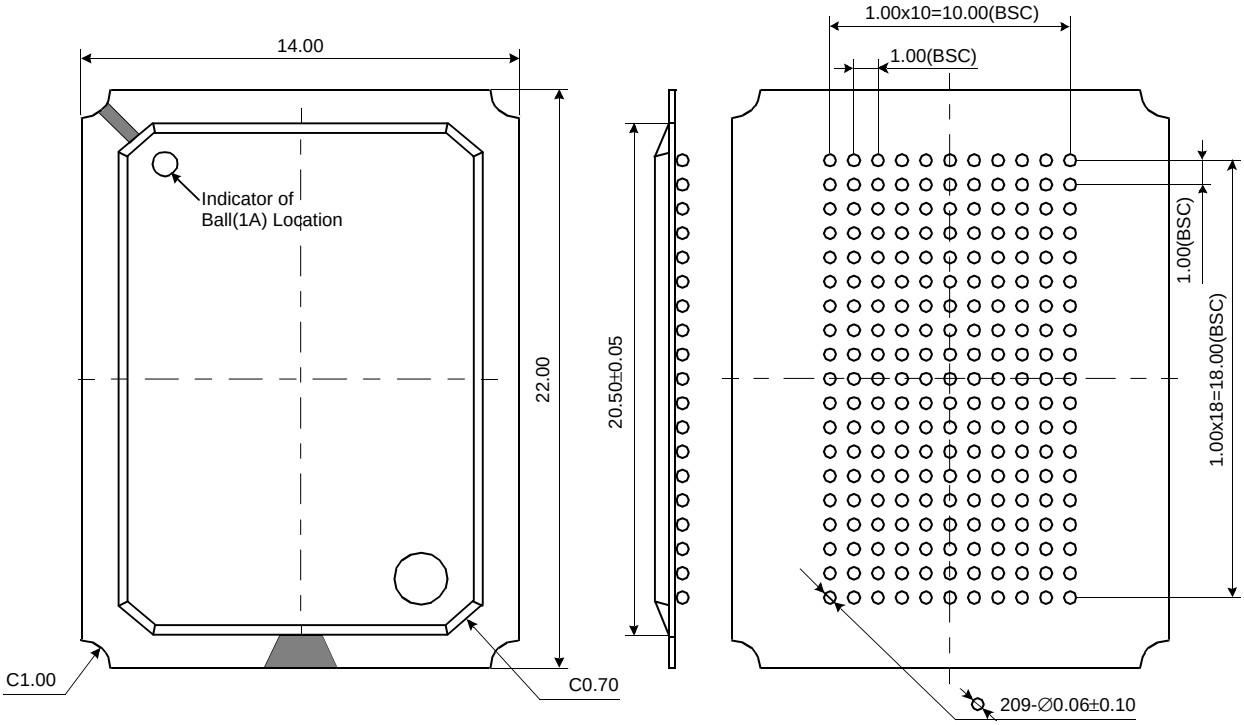
NOTE: $\overline{E1}$ does not deselect the Echo Clock Outputs. Echo Clock Outputs are de selected by E2 or E3 being sampled false.

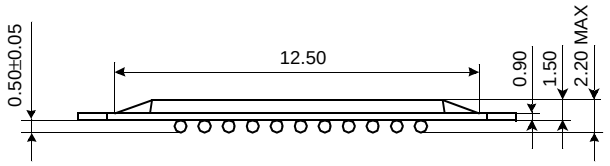
BANK SWITCH WITH $\overline{E1}$ DESELECT



209 Bump BGA PACKAGE DIMENSIONS

14mm x 22mm Body, 1.0mm Bump Pitch, 11x19 Bump Array





NOTE :
1. All Dimensions are in Millimeters.
2. Solder Ball to PCB Offset: 0.10 MAX.
3. PCB to Cavity Offset: 0.10 MAX.