

SN54HCT574, SN74HCT574 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS177C – MARCH 1984 – REVISED MAY 1997

- Inputs Are TTL-Voltage Compatible
- High-Current 3-State Noninverting Outputs Drive Bus Lines Directly or up to 15 LSTTL Loads
- Bus-Structured Pinout
- Package Options Include Plastic Small-Outline (DW), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

These octal edge-triggered D-type flip-flops feature 3-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

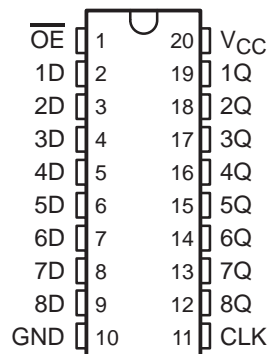
The eight flip-flops enter data on the low-to-high transition of the clock (CLK) input.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

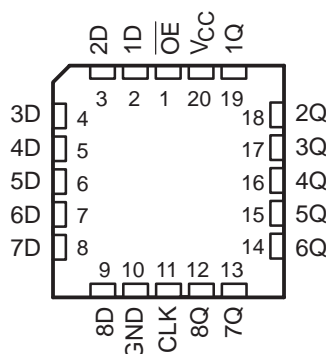
\overline{OE} does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HCT574 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HCT574 is characterized for operation from -40°C to 85°C .

SN54HCT574 . . . J OR W PACKAGE
SN74HCT574 . . . DW, N, OR PW PACKAGE
(TOP VIEW)



SN54HCT574 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT Q
\overline{OE}	CLK	D	
L	\uparrow	H	H
L	\uparrow	L	L
L	H or L	X	Q_0
H	X	X	Z



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**TEXAS
INSTRUMENTS**

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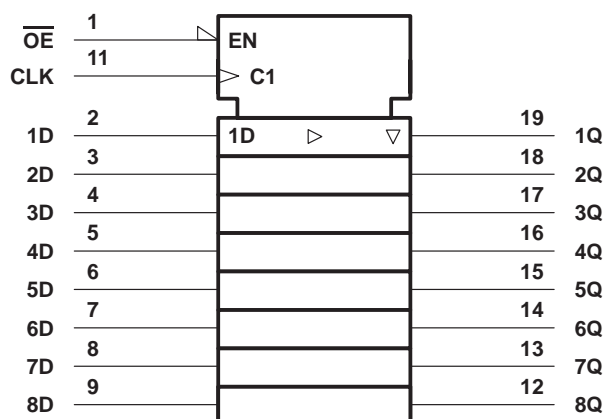
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OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

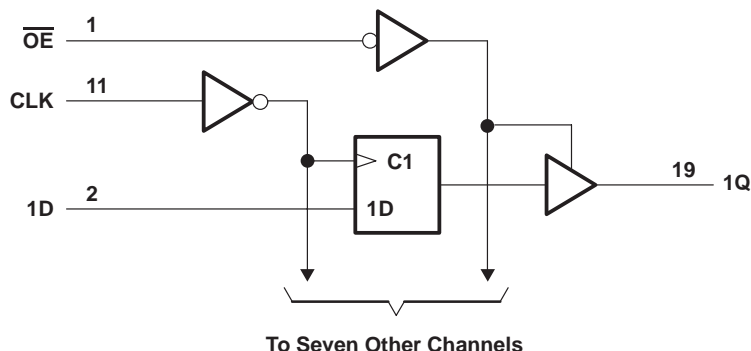
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND	± 70 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package	97°C/W
N package	67°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

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recommended operating conditions

			SN54HCT574			SN74HCT574			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 4.5 V to 5.5 V	2			2			V
V _{IL}	Low-level input voltage	V _{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V _I	Input voltage		0		V _{CC}	0		V _{CC}	V
V _O	Output voltage		0		V _{CC}	0		V _{CC}	V
t _t	Input transition (rise and fall) time		0		500	0		500	ns
T _A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HCT574		SN74HCT574		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = –20 µA	4.5 V	4.4	4.499		4.4		4.4		V
		I _{OH} = –6 mA		3.98	4.3		3.7		3.84		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 µA	4.5 V		0.001	0.1		0.1		0.1	V
		I _{OL} = 6 mA			0.17	0.26		0.4		0.33	
I _I	V _I = V _{CC} or 0		5.5 V	±0.1	±100		±1000		±1000		nA
I _{OZ}	V _O = V _{CC} or 0		5.5 V	±0.01	±0.5		±10		±5		µA
I _{CC}	V _I = V _{CC} or 0, I _O = 0		5.5 V			8	160		80		µA
ΔI _{CC} †	One input at 0.5 V or 2.4 V, Other inputs at 0 or V _{CC}		5.5 V		1.4	2.4	3		2.9		mA
C _i			4.5 V to 5.5 V		3	10	10		10		pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V _{CC}	T _A = 25°C		SN54HCT574		SN74HCT574		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	4.5 V	0	30	0	20	0	24	MHz
		5.5 V	0	33	0	22	0	27	
t _w	Pulse duration, CLK high or low	4.5 V	16		24		20		ns
		5.5 V	14		22		18		
t _{su}	Setup time, data before CLK↑	4.5 V	20		30		25		ns
		5.5 V	17		27		23		
t _h	Hold time, data after CLK↑	4.5 V	5		5		5		ns
		5.5 V	5		5		5		

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OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT574		SN74HCT574		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{\max}			4.5 V	30	36		20		24		MHz
			5.5 V	33	40		22		27		
t_{pd}	CLK	Any Q	4.5 V		30	36		54		45	ns
			5.5 V		25	32		48		41	
t_{en}	\overline{OE}	Any Q	4.5 V		26	30		45		38	ns
			5.5 V		23	27		41		34	
t_{dis}	\overline{OE}	Any Q	4.5 V		23	30		45		38	ns
			5.5 V		22	27		41		34	
t_t		Any Q	4.5 V		10	12		18		15	ns
			5.5 V		9	11		16		14	

switching characteristics over recommended operating free-air temperature range, $C_L = 150$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT574		SN74HCT574		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{\max}			4.5 V	30	36		20		24		MHz
			5.5 V	33	40		22		27		
t_{pd}	CLK	Any Q	4.5 V		40	53		80		66	ns
			5.5 V		35	47		71		60	
t_{en}	\overline{OE}	Any Q	4.5 V		34	47		71		59	ns
			5.5 V		29	39		94		78	
t_t		Any Q	4.5 V		18	42		63		53	ns
			5.5 V		16	38		57		48	

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	No load	93	pF

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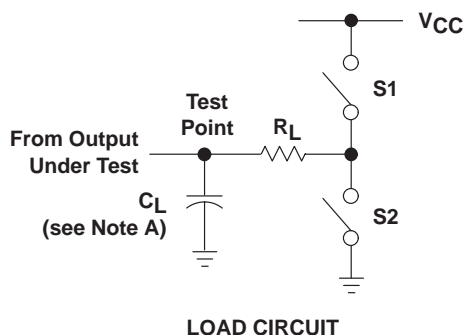


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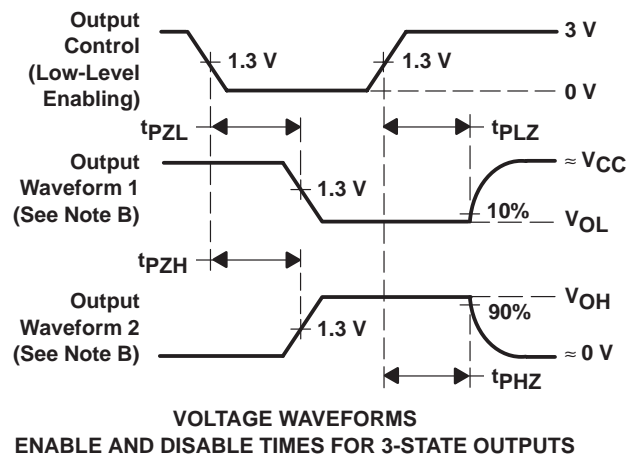
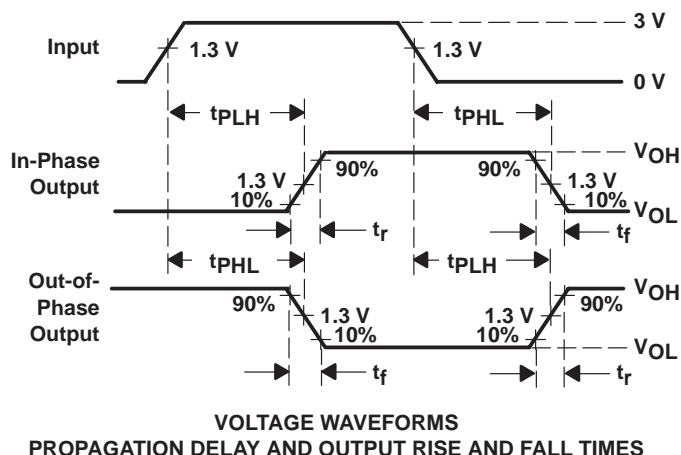
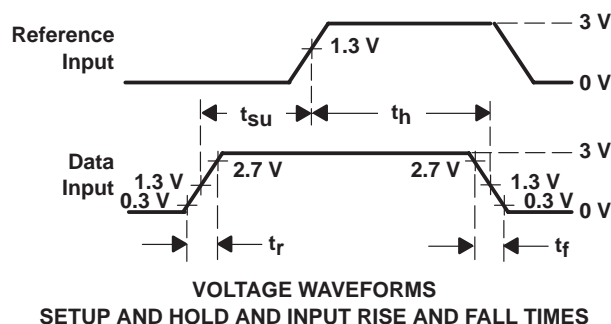
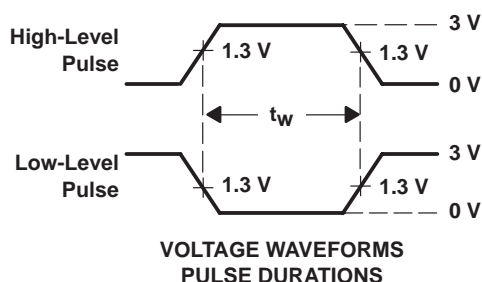
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PARAMETER MEASUREMENT INFORMATION



PARAMETER	R_L	C_L	S1	S2
t_{en}	1 k Ω	50 pF or 150 pF	Open	Closed
			Closed	Open
t_{dis}	1 k Ω	50 pF	Open	Closed
			Closed	Open
t_{pd} or t_t	—	50 pF or 150 pF	Open	Open



- NOTES: A. C_L includes probe and test-fixture capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
- D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
- E. The outputs are measured one at a time with one input transition per measurement.
- F. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- G. t_{PZL} and t_{PZH} are the same as t_{en} .
- H. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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