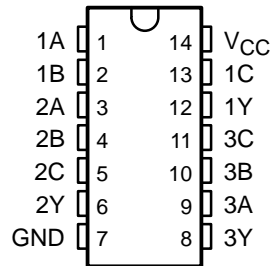


SN54ALS11A, SN54AS11, SN74ALS11A, SN74AS11 TRIPLE 3-INPUT POSITIVE-AND GATES

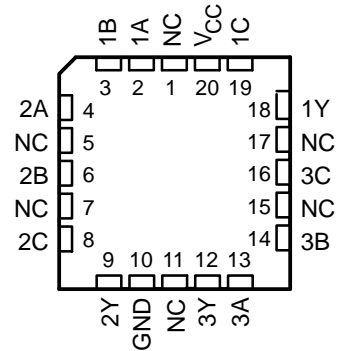
SDAS009D – MARCH 1984 – REVISED NOVEMBER 2002

- 4.5-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 5.5 ns at 5 V

SN54ALS11A, ... J OR W PACKAGE
SN54AS11 ... J PACKAGE
SN74ALS11A, SN74AS11 ... D, N, OR NS PACKAGE
(TOP VIEW)



SN54ALS11A, SN54AS11 ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These devices contain three independent 3-input positive-AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74ALS11AN	SN74ALS11AN
			SN74AS11N	SN74AS11N
	SOIC – D	Tube	SN74ALS11AD	ALS11A
		Tape and reel	SN74ALS11ADR	
		Tube	SN74AS11D	AS11
		Tape and reel	SN74AS11DR	
	SOP – NS	Tape and reel	SN74ALS11ANSR	ALS11A
			SN74AS11NSR	74AS11
–55°C to 125°C	CDIP – J	Tube	SNJ54ALS11AJ	SNJ54ALS11AJ
			SNJ54AS11J	SNJ54AS11J
	CFP – W	Tube	SNJ54ALS11AW	SNJ54ALS11AW
	LCCC – FK	Tube	SNJ54ALS11AFK	SNJ54ALS11AFK
			SNJ54AS11FK	SNJ54AS11FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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**TEXAS
INSTRUMENTS**

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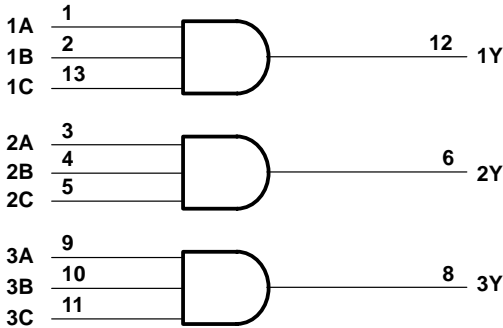
SN54ALS11A, SN54AS11, SN74ALS11A, SN74AS11
TRIPLE 3-INPUT POSITIVE-AND GATES

SDAS009D – MARCH 1984 – REVISED NOVEMBER 2002

FUNCTION TABLE
(each gate)

INPUTS			OUTPUT Y
A	B	C	
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

logic diagram, each gate (positive logic)



Pin numbers shown are for the D, J, N, NS, and W packages.

absolute maximum ratings over operating free-air temperature range (SN54ALS11A, SN74ALS11A) (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Package thermal impedance, θ_{JA} (see Note 1): D package	86°C/W
N package	80°C/W
NS package	76°C/W
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

		SN54ALS11A			SN74ALS11A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8 [‡]			0.8	V
				0.7 [§]				
I_{OH}	High-level output current			–0.4			–0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

[‡] Applies over temperature range –55°C to 70°C

[§] Applies over temperature range 70°C to 125°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54ALS11A, SN54AS11, SN74ALS11A, SN74AS11 TRIPLE 3-INPUT POSITIVE-AND GATES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS11A		SN74ALS11A		UNIT
			MIN	TYP†	MAX	MIN	
V _{IK}	V _{CC} = 4.5 V, I _I = −18 mA		−1.5		−1.5		V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = −0.4 mA		V _{CC} − 2		V _{CC} − 2		V
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 4 mA	0.25	0.4	0.25	0.4	V
		I _{OL} = 8 mA			0.35	0.5	
I _I	V _{CC} = 5.5 V, V _I = 7 V		0.1		0.1		mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V		20		20		μA
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V		−0.1		−0.1		mA
I _O [‡]	V _{CC} = 5.5 V, V _O = 2.25 V		−20	−112	−30	−112	mA
I _{CCH}	V _{CC} = 5.5 V, V _I = 4.5 V		1	1.8	1	1.8	mA
I _{CCL}	V _{CC} = 5.5 V, V _I = 0		1.6	3	1.6	3	mA

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V TO 5.5 V, C _L = 50 PF, R _L = 500 Ω, T _A = MIN TO MAX§				UNIT
			SN54ALS11A		SN74ALS11A		
			MIN	MAX	MIN	MAX	
t _{PLH}	A, B, or C	Y	2	14	2	13	ns
t _{PHL}			2	12.5	2	10	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**absolute maximum ratings over operating free-air temperature range (SN54AS11, SN74AS11)
(unless otherwise noted)¶**

Supply voltage, V_{CC} 7 V

Input voltage, V_I 7 V

Package thermal impedance, θ_{JA} (see Note 1): D package 86°C/W

N package 80°C/W

NS package 76°C/W

Storage temperature range -65°C to 150°C

¶ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

SN54ALS11A, SN54AS11, SN74ALS11A, SN74AS11

TRIPLE 3-INPUT POSITIVE-AND GATES

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recommended operating conditions (see Note 2)

		SN54AS11			SN74AS11			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			–2			–2	mA
I _{OL}	Low-level output current			20			20	mA
T _A	Operating free-air temperature	–55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS11			SN74AS11			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = –18 mA			–1.2			–1.2	V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = –2 mA	V _{CC} –2			V _{CC} –2			V
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I _I	V _{CC} = 5.5 V, V _I = 7 V			0.1			0.1	mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V			20			20	μA
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V			–0.5			–0.5	mA
I _O ‡	V _{CC} = 5.5 V, V _O = 2.25 V	–30		–112	–30		–112	mA
I _{CCH}	V _{CC} = 5.5 V, V _I = 4.5 V		4.3	7		4.3	7	mA
I _{CCL}	V _{CC} = 5.5 V, V _I = 0		11.2	18		11.2	18	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS}.

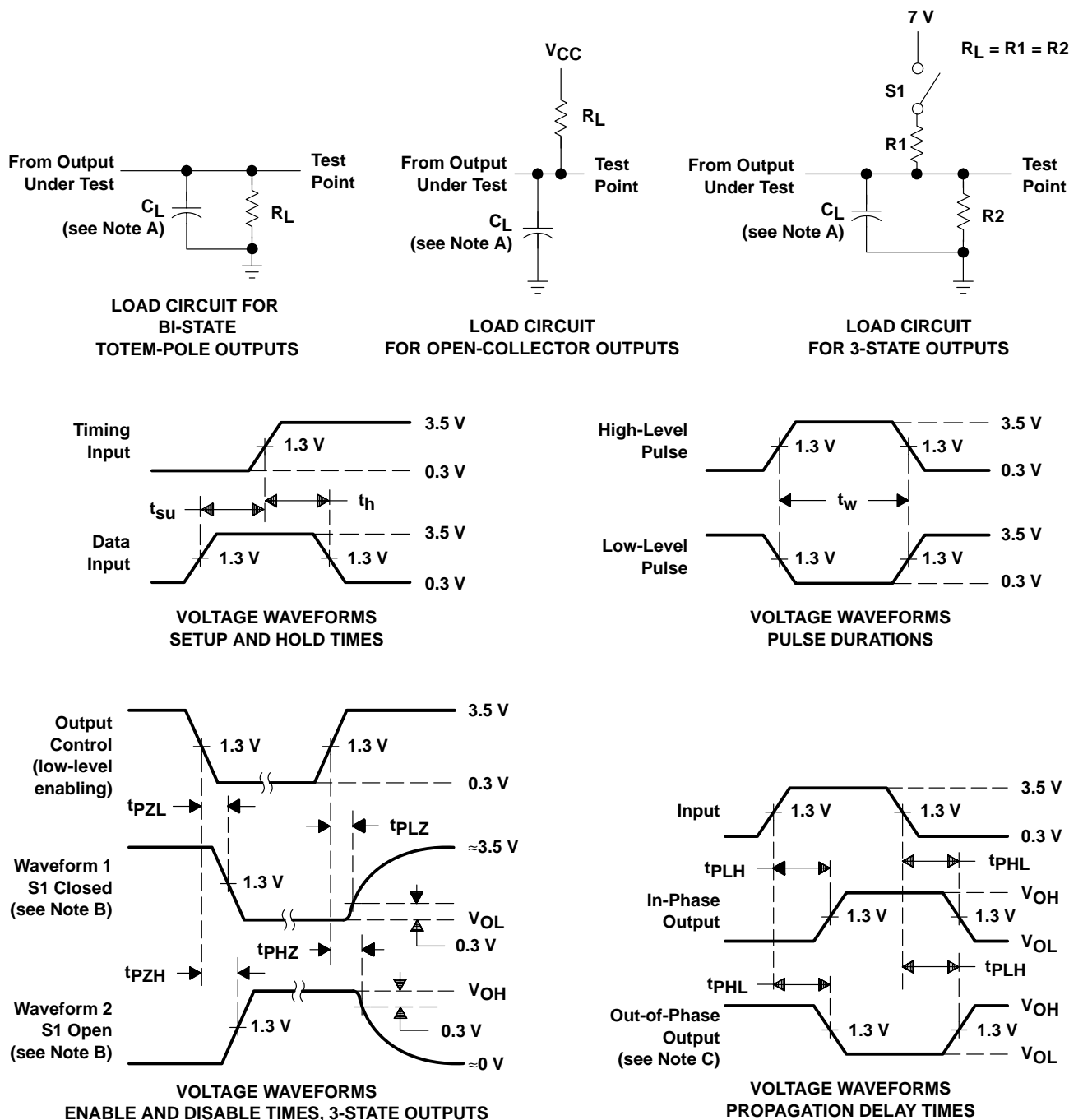
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V TO 5.5 V, C _L = 50 PF, R _L = 500 Ω, T _A = MIN TO MAX§				UNIT
			SN54AS11		SN74AS11		
			MIN	MAX	MIN	MAX	
t _{PLH}	A, B, or C	Y	1	6.5	1	6	ns
t _{PHL}			1	6.5	1	5.5	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



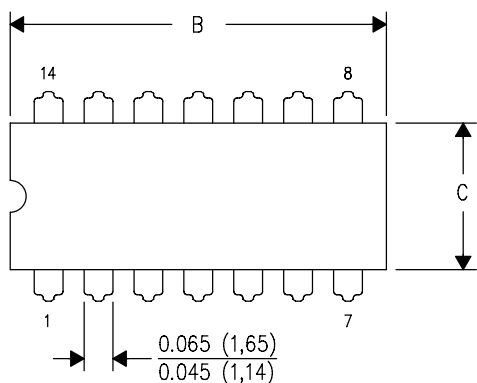
- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

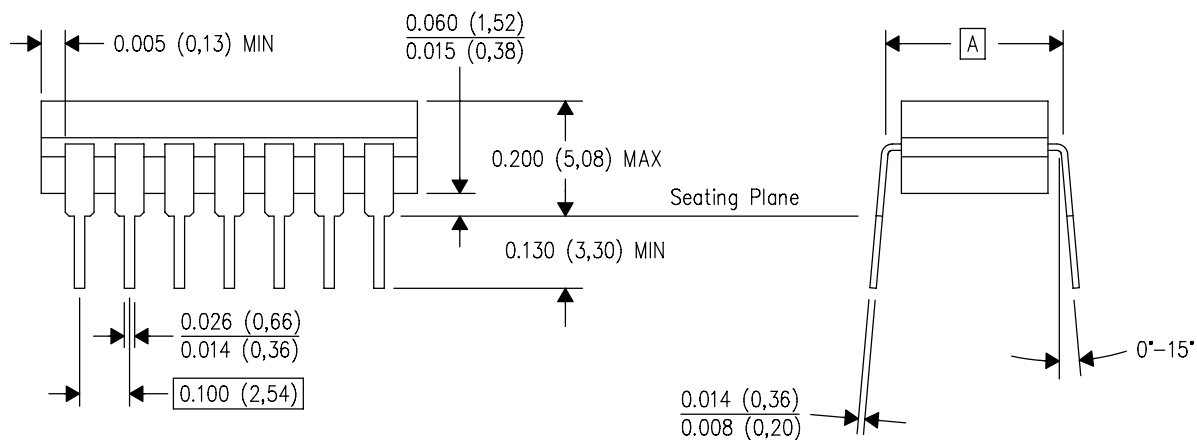
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

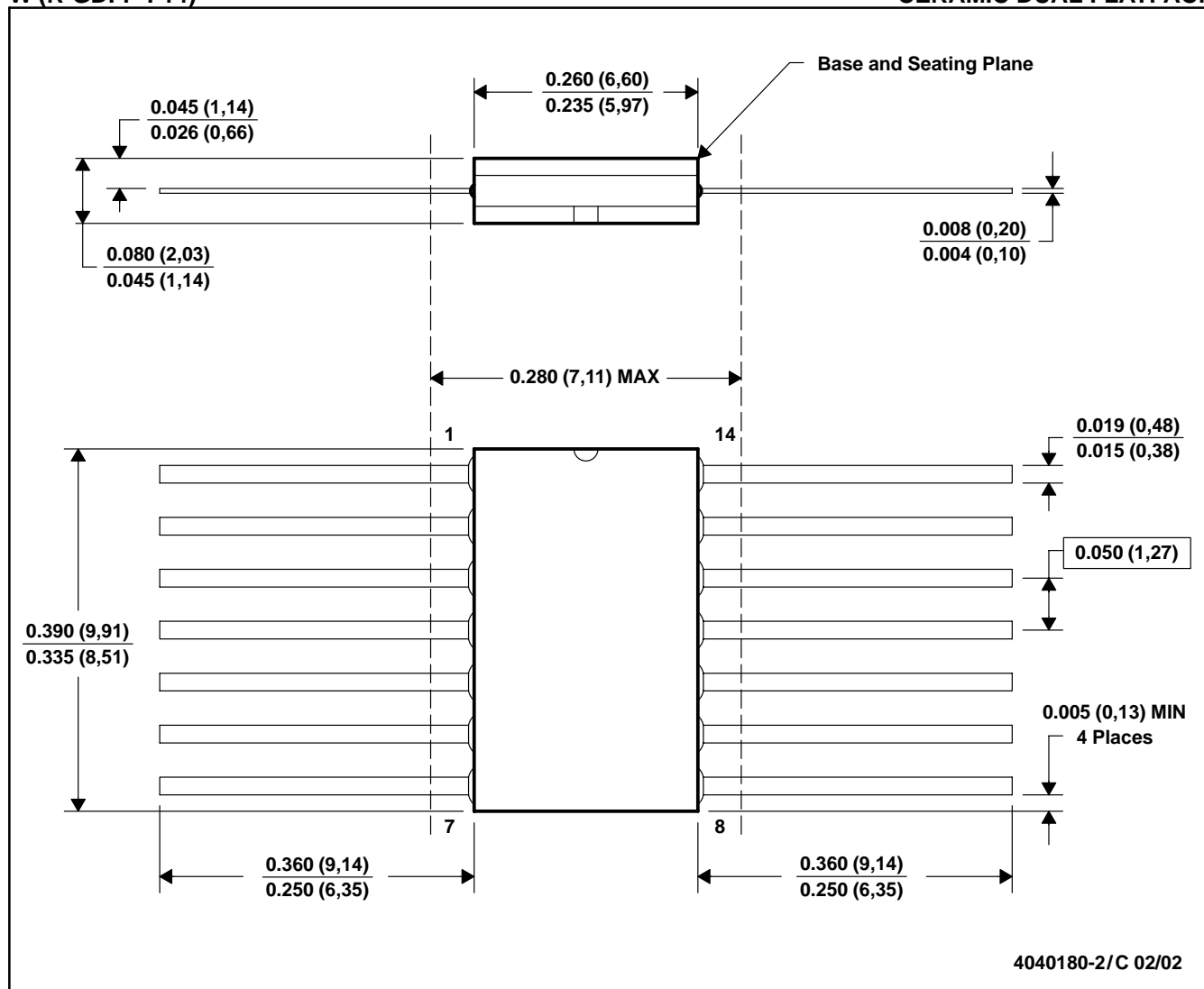


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK

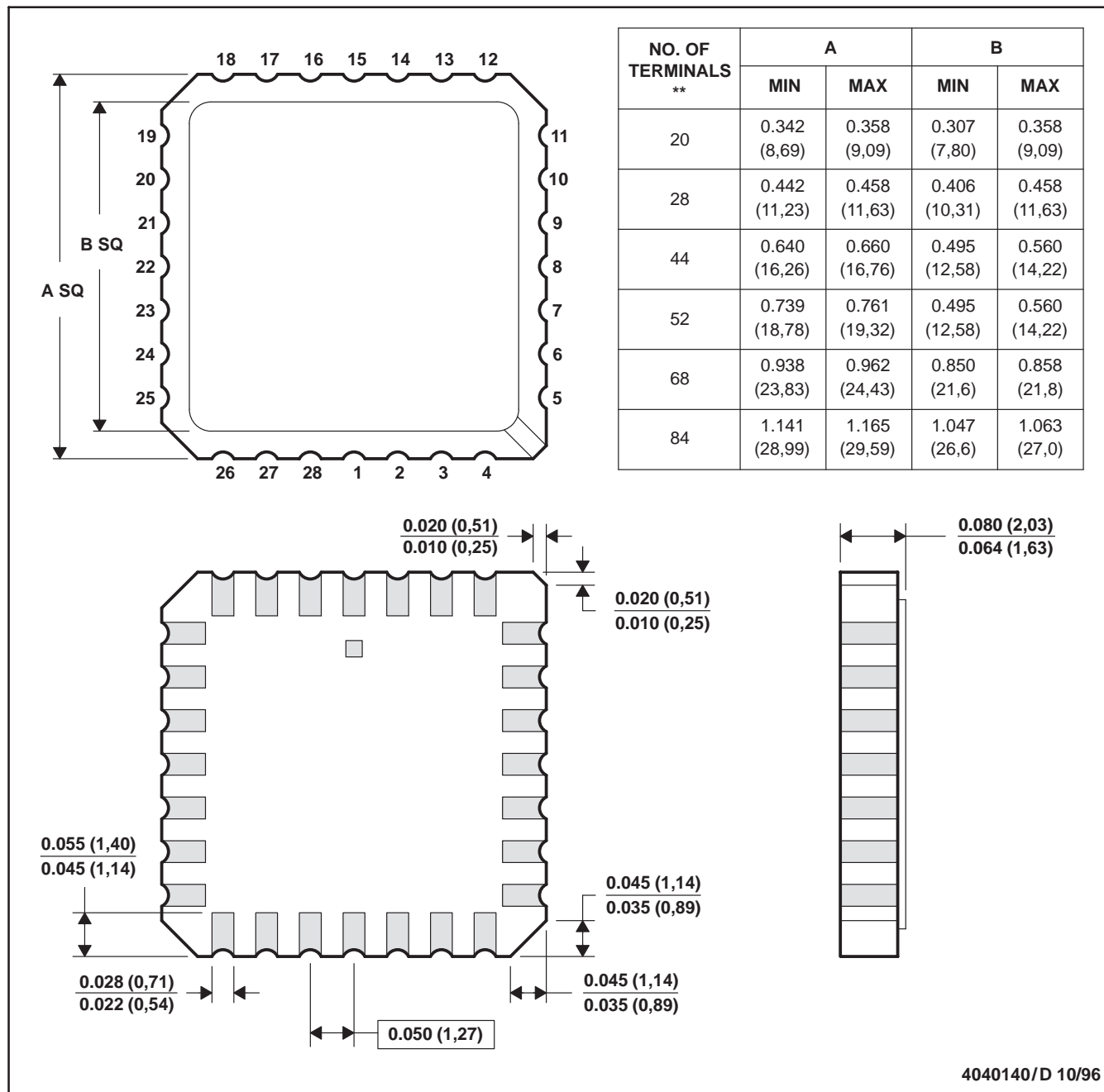


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

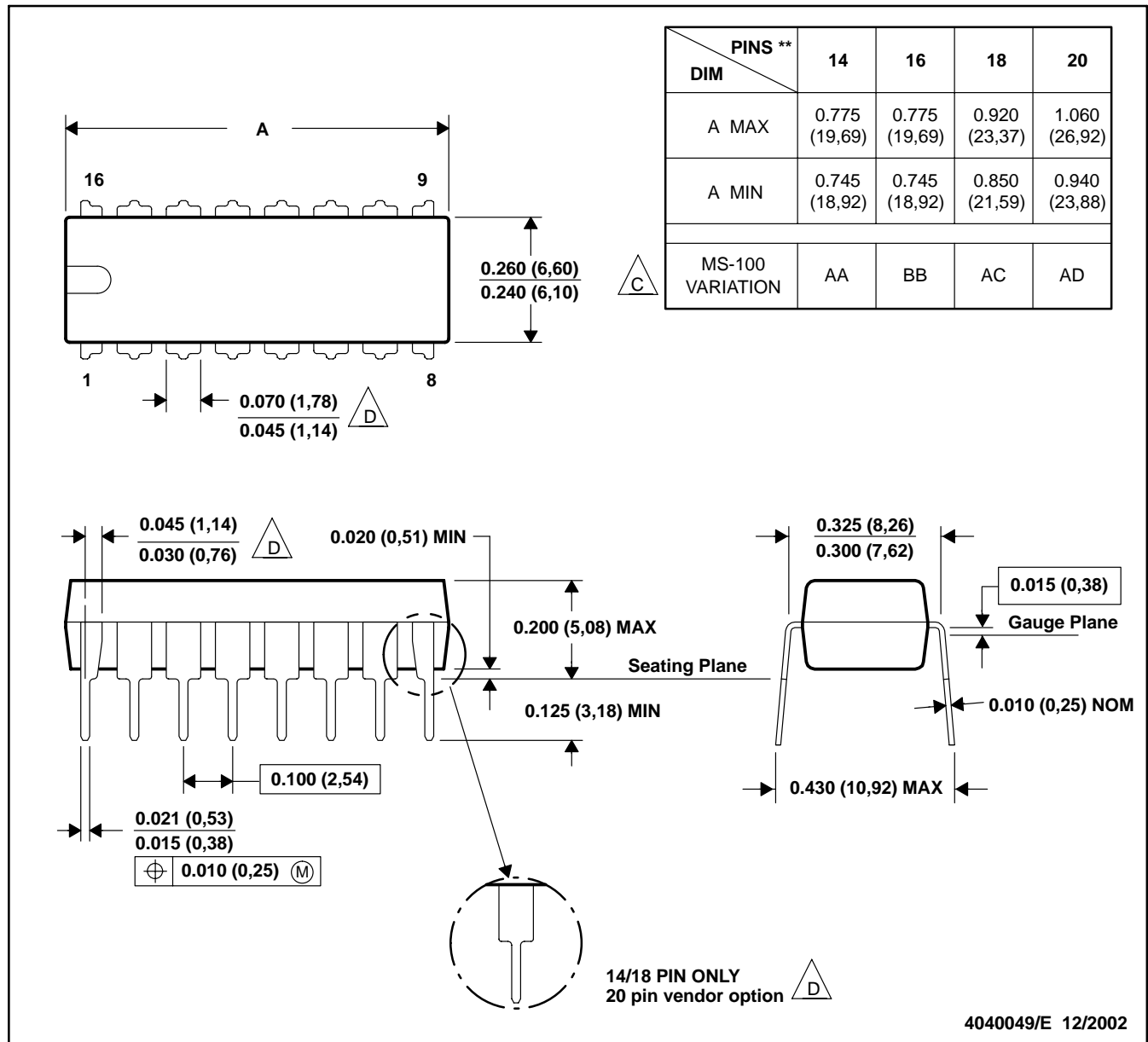
28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T)**

16 PINS SHOWN

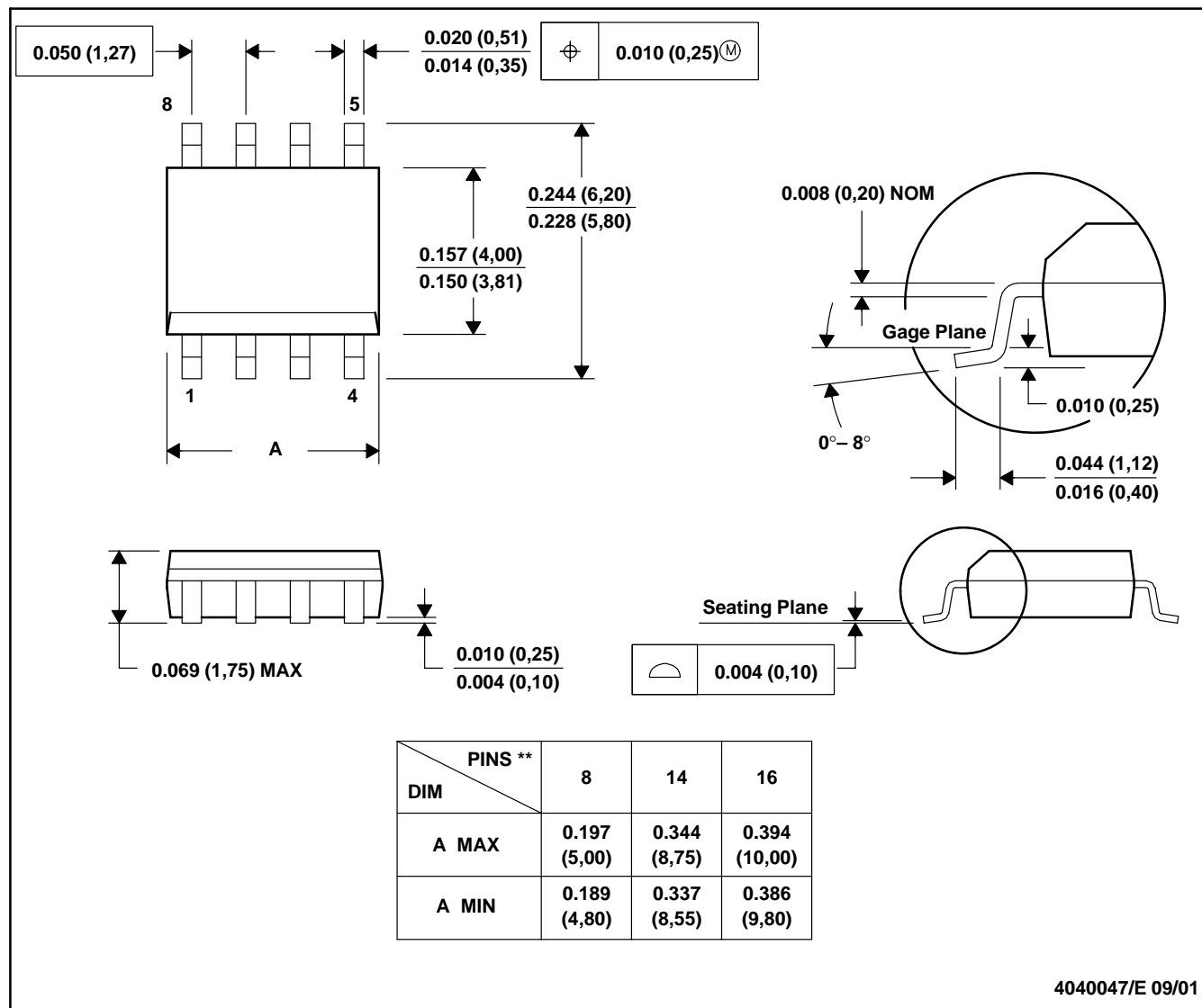
PLASTIC DUAL-IN-LINE PACKAGE

NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G)****PLASTIC SMALL-OUTLINE PACKAGE****8 PINS SHOWN**

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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