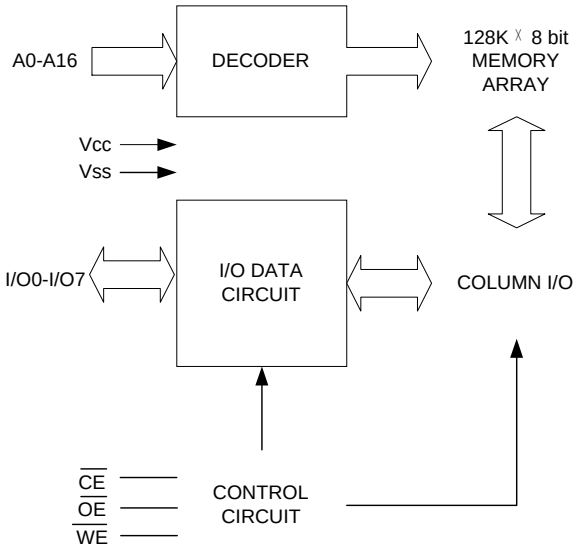
REVISION HISTORY

REVISION	DESCRIPTION	Date
Preliminary Rev. 0.1	Original.	Jan 2,2002
Rev. 1.0	1.Revised CMOS low power operating : Operating current : 195→150mA (max.) Standby current : 30mA (max.) →1mA(Typ.) 2.Revised power supply : 3.0~3.6V→3.15~3.6V 3.Revised DC CHARACTERISTICE I_{CC} –8ns (max) : 200→150mA I_{CC} –10ns (max) : 195→120mA I_{CC} –12ns (max) : 190→100mA I_{CC} –15ns (max) : 150→80 mA I_{SB} (max) : 30→10mA, I_{SB} (typ) : NA→3mA I_{SB1} (max) : 10→3mA, I_{SB1} (typ) : NA→1mA I_{SB1} (max)<1 mA for special order 4. Add order information for lead free product	May 20,2003

FEATURES

- Fast access time :
  8ns for Vcc=3.15V~3.6V
  10/12/15ns for Vcc=3.0V~3.6V
- CMOS low power operating :
  Operating current : 150mA (max.)
  Standby current : 1mA (Typ.)
- Single 3.15~3.6V power supply
- Operating temperature :
  Commercial : 0℃~70℃
- All TTL compatible inputs and outputs
- Fully static operation
- Three state outputs
- Package : 32-pin 8mm x 13.4mm STSOP

FUNCTIONAL BLOCK DIAGRAM



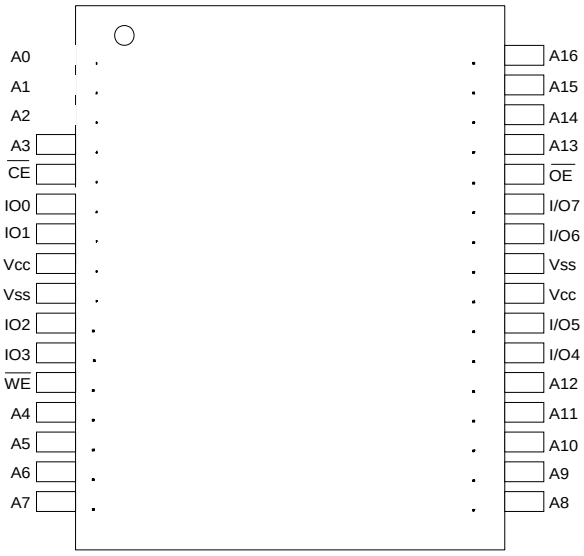
GENERAL DESCRIPTION

The UT61L1288 is a 1,048,576-bit high-speed CMOS static random access memory organized as 131,072 words by 8 bits.

The UT61L1288 operates from a single 3.15~3.6V power supply and all inputs and outputs are fully TTL compatible.

It is fabricated using high performance, high reliability CMOS technology.

PIN CONFIGURATION



STSOP

PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A16	Address Inputs
I/O0 - I/O7	Data Inputs/Outputs
$\overline{CE}$	Chip enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS*

PARAMETER		SYMBOL	RATING	UNIT
Terminal Voltage with Respect to Vss		V_{TERM}	-0.5 to 4.6	V
Operating Temperature	Commercial	T_A	0 to 70	℃
Storage Temperature		T_{STG}	-65 to 150	℃
Power Dissipation		P_D	1	W
DC Output Current		I_{OUT}	50	mA
Soldering Temperature (under 10 secs)		Tsolder	260	℃

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High - Z	I_{SB},I_{SB1}
Output Disable	L	H	H	High - Z	I_{CC}
Read	L	L	H	D_{OUT}	I_{CC}
Write	L	X	L	D_{IN}	I_{CC}

Note: H = V_{IH}, L=V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS (T_A = 0℃ to 70℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Power Voltage	V_{CC}		8	3.15	3.3	3.6	V
			10/12/15	3.0	3.3	3.6	V
Input High Voltage	V_{IH}			2.0	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}			-0.3	-	0.8	V
Input Leakage Current	I_{LI}	$V_{SS} \leqq V_{IN} \leqq V_{CC}$		- 2	-	2	μA
Output Leakage Current	I_{LO}	$V_{SS} \leqq V_{I/O} \leqq V_{CC}$; Output Disable		- 2	-	2	μA
Output High Voltage	V_{OH}	I_{OH}= -4mA		2.4	-	-	V
Output Low Voltage	V_{OL}	I_{OL}= 8mA		-	-	0.4	V
Operating Power Supply Current	I_{CC}	Cycle time=min, 100%duty I/O=0mA, $\overline{CE}$ =V_{IL}	8	-	-	150	mA
			10	-	-	120	mA
			12	-	-	100	mA
			15	-	-	80	mA
Standby Current (TTL)	I_{SB}	$\overline{CE}$ =V_{IH}, other pins =V_{IL} or V_{IH}		-	3	10	mA
Standby Current (CMOS)	I_{SB1}	$\overline{CE}$ =V_{CC}-0.2V, other pins at 0.2V or Vcc-0.2V		-	1	3*[4]	mA

Notes:
1. Overshoot : Vcc+3.0v for pulse width less than 6ns.
2. Undershoot : Vss-3.0v for pulse width less than 6ns.
3. Overshoot and Undershoot are sampled, not 100% tested.
4. I_{SB1}< 1mA for special order or requirement.

CAPACITANCE (T_A=25℃, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L=30pF, I_{OH}/I_{OL}= -4mA / 8mA

AC ELECTRICAL CHARACTERISTICS (T_A = 0℃ to 70℃)

(1) READ CYCLE

PARAMETER	SYMBOL	UT61L1288 -8 V_{CC}=3.15 3.6		UT61L1288 -10 V_{CC}=3.0 3.6		UT61L1288 -12 V_{CC}=3.0 3.6		UT61L1288 -15 V_{CC}=3.0 3.6		UNIT
		MIN.	MAX.	MIN.	MIN.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	8	-	10	-	12	-	15	-	ns
Address Access Time	t_{AA}	-	8	-	10	-	12	-	15	ns
Chip Enable Access Time	t_{ACE}	-	8	-	10	-	12	-	15	ns
Output Enable Access Time	t_{OE}	-	4	-	5	-	6	-	7	ns
Chip Enable to Output in Low Z	t_{CLZ*}	3	-	3	-	3	-	3	-	ns
Output Enable to Output in Low Z	t_{OLZ*}	0	-	0	-	0	-	0	-	ns
Chip Disable to Output in High Z	t_{CHZ*}	-	4	-	5	-	6	-	7	ns
Output Disable to Output in High Z	t_{OHZ*}	-	4	-	5	-	6	-	7	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	3	-	ns

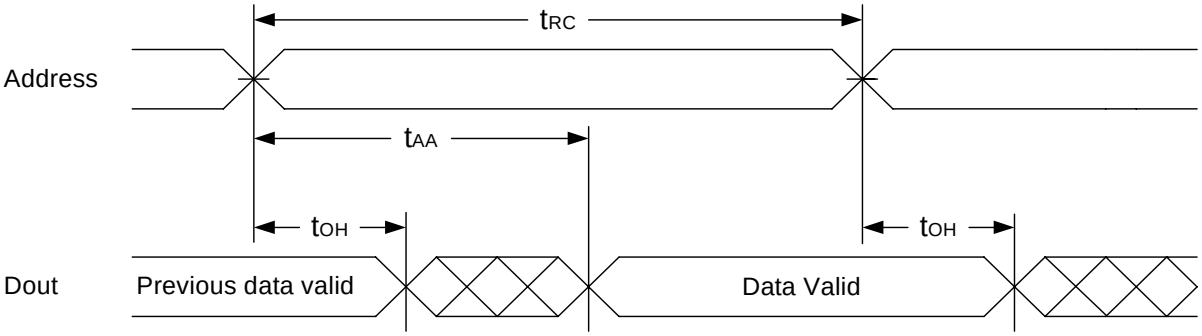
(2) WRITE CYCLE

PARAMETER	SYMBOL	UT61L1288 -8 V_{CC}=3.15 3.6		UT61L1288 -10 V_{CC}=3.0 3.6		UT61L1288 -12 V_{CC}=3.0 3.6		UT61L1288 -15 V_{CC}=3.0 3.6		UNIT
		MIN.	MAX.	MIN.	MIN.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	8	-	10	-	12	-	15	-	ns
Address Valid to End of Write	t_{AW}	7	-	8	-	9	-	10	-	ns
Chip Enable to End of Write	t_{CW}	7	-	8	-	9	-	10	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	7	-	8	-	9	-	10	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	5.5	-	6	-	7	-	8	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW*}	3	-	3	-	3	-	3	-	ns
Write to Output in High Z	t_{WHZ*}	-	4	-	5	-	6	-	7	ns

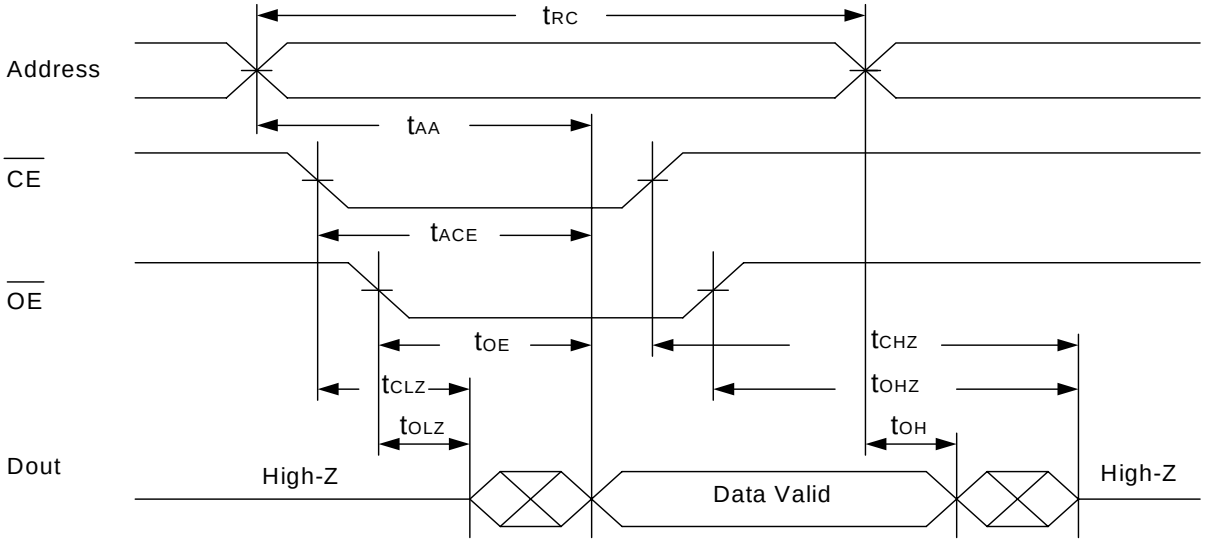
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



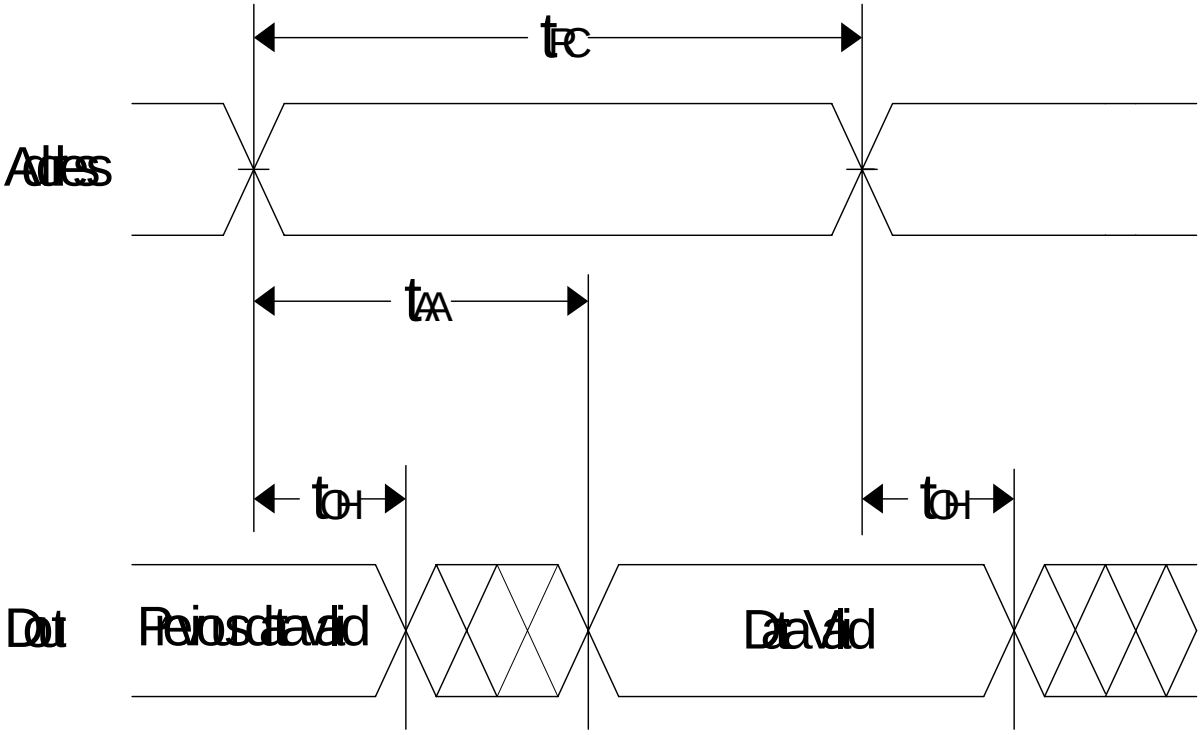
READ CYCLE 2 ($\overline{CE}$ and $\overline{OE}$ Controlled) (1,3,4,5)



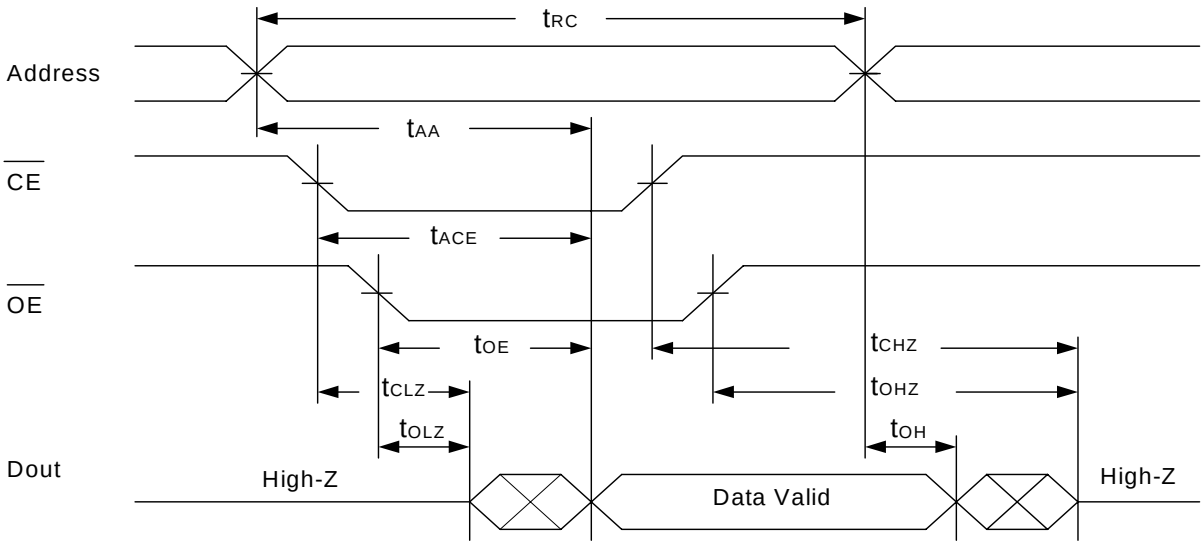
Notes :

1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected $\overline{OE}$ =low, $\overline{CE}$ =low.
3. Address must be valid prior to or coincident with $\overline{CE}$ =low,; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ}, t_{OLZ}, t_{CHZ} and t_{OHZ} are specified with C_L=5pF. Transition is measured ±500mV from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ}, t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 ($\overline{WE}$ Controlled) (1,2,3,5,6)



WRITE CYCLE 2 ($\overline{CE}$ Controlled) (1,2,5,6)

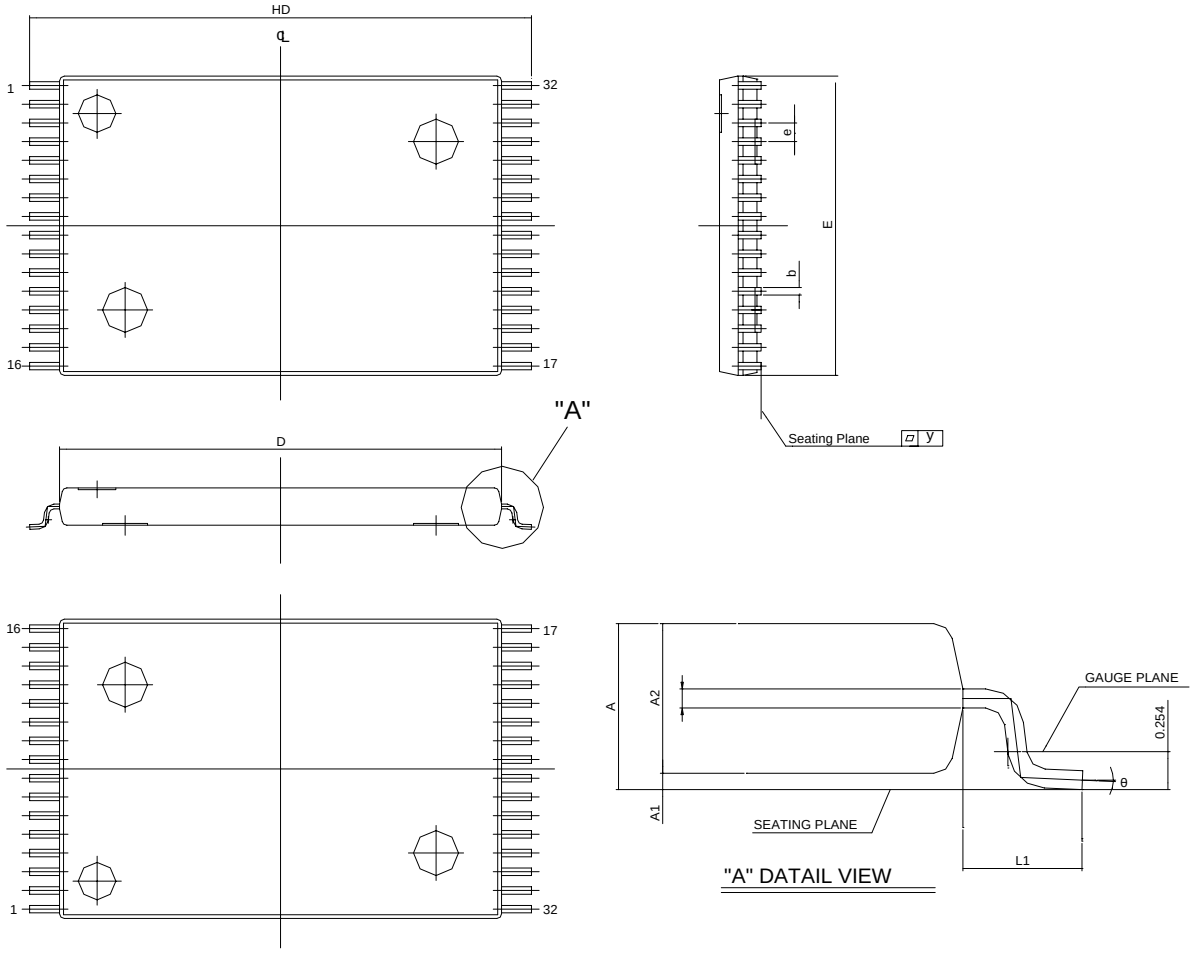


Notes :

1. $\overline{WE}$, $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap of a low $\overline{CE}$, low $\overline{WE}$.
3. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ low, t_{WP} must be greater than $t_{WHZ}+t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured $\pm$500mV from steady state.

PACKAGE OUTLINE DIMENSION

32-pin 8mm x 13.4mm STSOP Package Outline Dimension



SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004 ±0.002	0.10 ±0.05
A2	0.039 ±0.002	1.00 ±0.05
b	0.008 ±0.001	0.200 ±0.025
D	0.465 ±0.004	11.800 ±0.100
E	0.315 ±0.004	8.000 ±0.100
e	0.020 (TYP)	0.50 (TYP)
HD	0.528 ±0.008	13.40 ±0.20.
L1	0.0315 ±0.004	0.80 ±0.10
y	0.003 (MAX)	0.076 (MAX)
θ	0^o 5^o	0^o 5^o

ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	PACKAGE
UT61L1288LS-8	8	32 PIN STSOP
UT61L1288LS-10	10	32 PIN STSOP
UT61L1288LS-12	12	32 PIN STSOP
UT61L1288LS-15	15	32 PIN STSOP

ORDERING INFORMATION (for lead free product)

PART NO.	ACCESS TIME (ns)	PACKAGE
UT61L1288LSL-8	8	32 PIN STSOP
UT61L1288LSL-10	10	32 PIN STSOP
UT61L1288LSL-12	12	32 PIN STSOP
UT61L1288LSL-15	15	32 PIN STSOP

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