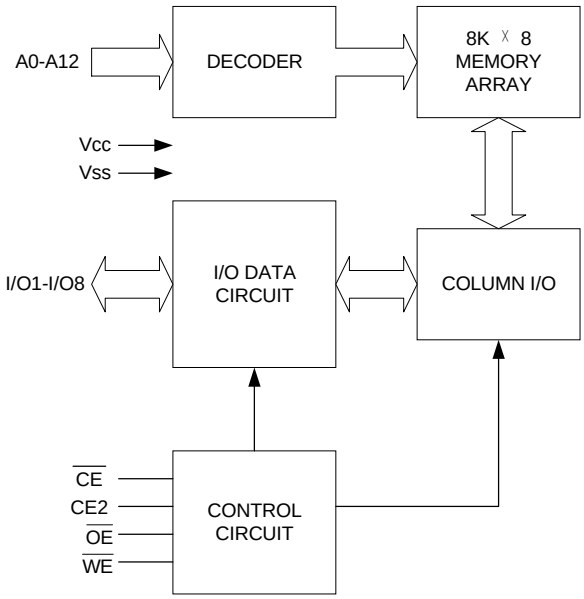
REVISION HISTORY

REVISION	DESCRIPTION	Released Date
Rev. 0.1	Original	May 3,2001
Rev. 1.0	Release	Feb.26,2002
Rev. 1.1	Revised - Improve I_{DR} from 20μA to 10μA (LL-version , max.)	May 14,2002
Rev. 1.2	1. Revised Single power supply : 3.3V→3.0V~3.6V 2. Add Extended temperature : -20℃~85℃ 3. Revised "Order information" : add Extended parts 4. AC/DC characteristics : -add Extended temperature -Icc1 (TYP):12→6mA, Icc1 (MAX) : 20→10mA -Icc2 (TYP):6→12mA, Icc2(MAX) : 10→20mA	Jul 30,2002
Rev. 1.3	Add order information for lead free product	May 15,2003

FEATURES

- Access time : 35/70ns (max.)
- Low power consumption:
  Operating : 30/20 mA (typical)
  Standby : 1.5mA (typical) normal
  1 μA (typical) L-version
  0.5 μA (typical) LL-version
- Single 3.0V~3.6V power supply
- Operating temperature :
  Commerical : 0℃~70℃
  Extended : -20℃~85℃
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Data retention voltage : 1.5V (min.)
- Package : 28-pin 600mil PDIP
  28-pin 330 mil SOP
- Substrate connected : Vcc

FUNCTIONAL BLOCK DIAGRAM

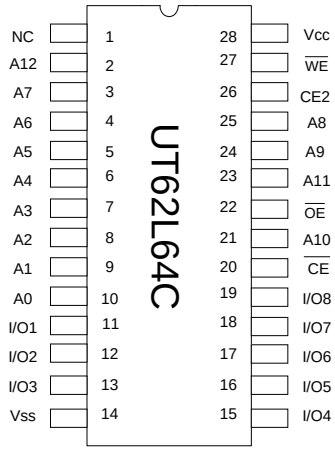


GENERAL DESCRIPTION

The UT62L64C is a 65,536-bits low power CMOS static random access memory organized as 8,192 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

Easy memory expansion is provided by using two chip enable input.($\overline{CE}$,CE2) The UT62L64C operates from a single 3.3V power supply and all inputs and outputs are fully TTL compatible.

PIN CONFIGURATION



SOP/PDIP

PAD DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A12	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
$\overline{CE}$,CE2	Chip Enable Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	Power Supply
V_{SS}	Ground
NC	

ABSOLUTE MAXIMUM RATINGS*

PARAMETER		SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V_{SS}		V_{TERM}	-0.5 to 4.5	V
Operating Temperature	Commerical	T_A	0 to 70	℃
	Extended	T_A	-20 to 85	℃
Storage Temperature		T_{STG}	-65 to 150	℃
Power Dissipation		P_D	1	W
DC Output Current		I_{OUT}	50	mA
Soldering Temperature (under 10 sec)		Tsolder	260	℃

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	$\overline{CE}$	CE2	$\overline{OE}$	$\overline{WE}$	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High - Z	I_{SB}, I_{SB1}
Standby	X	L	X	X	High - Z	I_{SB}, I_{SB1}
Output Disable	L	H	H	H	High - Z	I_{CC}, I_{CC1}, I_{CC2}
Read	L	H	L	H	D_{OUT}	I_{CC}, I_{CC1}, I_{CC2}
Write	L	H	X	L	D_{IN}	I_{CC}, I_{CC1}, I_{CC2}

note: H = V_{IH}, L=V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.0~3.6V, T_A = 0℃ to 70℃ / -20℃ to 85℃(E))

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Input High Voltage	V_{IH}*1			2.2	-	VCC+0.5	V
Input Low Voltage	V_{IL}*2			- 0.5	-	0.6	V
Input Leakage Current	I_{LI}	$V_{SS} \leqq V_{IN} \leqq V_{CC}$		- 1	-	1	μA
Output Leakage Current	I_{LO}	$V_{SS} \leqq V_{I/O} \leqq V_{CC}$ $\overline{CE}$ = V_{IH} or CE2= V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}		- 1	-	1	μA
Output High Voltage	V_{OH}	I_{OH} = - 1mA		2.4	-	-	V
Output Low Voltage	V_{OL}	I_{OL} = 4mA		-	-	0.4	V
Operating Power Supply Current	I_{CC}	Cycle time=Min, $I_{I/O}$ = 0mA $\overline{CE}$ = V_{IL} , CE2= V_{IH}	- 35	-	30	40	mA
			- 70	-	20	30	mA
	Icc1	$\overline{CE}$ =0.2V; $I_{I/O}$= 0mA other pins at 0.2V or Vcc-0.2V;	TCycle =1us	-	6	10	mA
	Icc2	$\overline{CE}$ =0.2V; $I_{I/O}$= 0mA other pins at 0.2V or Vcc-0.2V	TCycle =500ns	-	12	20	mA
Standby Current (TTL)	I_{SB}	$\overline{CE}$ = V_{IH} or CE2= V_{IL} other pins=V_{IL} or V_{IH}	Normal	-	1	10	mA
			- L/- LL	-	0.3	3	mA
Standby current (CMOS)	I_{SB1}	$\overline{CE} \geqq V_{CC}$-0.2V or CE2$\leqq$ 0.2V , other pins at 0.2V or Vcc-0.2V	Normal	-	1.5	5	mA
			- L		1	100	μA
			- LL	-	0.5	50	μA

Notes:
1. Overshoot : Vcc+3.0v for pulse width less than 10ns.
2. Undershoot : Vss-3.0v for pulse width less than 10ns.
3. Overshoot and Undershoot are sampled, not 100% tested.

CAPACITANCE (T_A=25°C, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 100pF, I_{OH}/I_{OL} = -1mA/4 mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.0~3.6V, T_A = 0°C to 70°C / -20°C to 85°C(E))

(1) READ CYCLE

PARAMETER	SYMBOL	UT62L64C-35		UT62L64C-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	35	-	70	-	ns
Address Access Time	t_{AA}	-	35	-	70	ns
Chip Enable Access Time	t_{ACE}	-	35	-	70	ns
Output Enable Access Time	t_{OE}	-	25	-	35	ns
Chip Enable to Output in Low-Z	t_{CLZ*}	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ*}	5	-	5	-	ns
Chip Disable to Output in High-Z	t_{CHZ*}	-	25	-	35	ns
Output Disable to Output in High-Z	t_{OHZ*}	-	25	-	35	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	ns

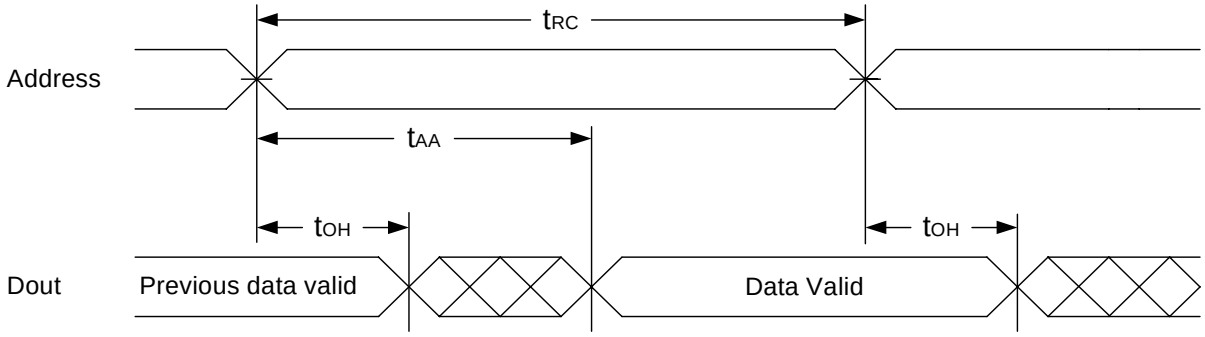
(2) WRITE CYCLE

PARAMETER	SYMBOL	UT62L64C-35		UT62L64C-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	35	-	70	-	ns
Address Valid to End of Write	t_{AW}	30	-	60	-	ns
Chip Enable to End of Write	t_{CW}	30	-	60	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	ns
Write Pulse Width	t_{WP}	25	-	50	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	20	-	30	-	ns
Data Hold from End of Write-Time	t_{DH}	0	-	0	-	ns
Output Active from End of Write	t_{OW*}	5	-	5	-	ns
Write to Output in High-Z	t_{WHZ*}	-	15	-	25	ns

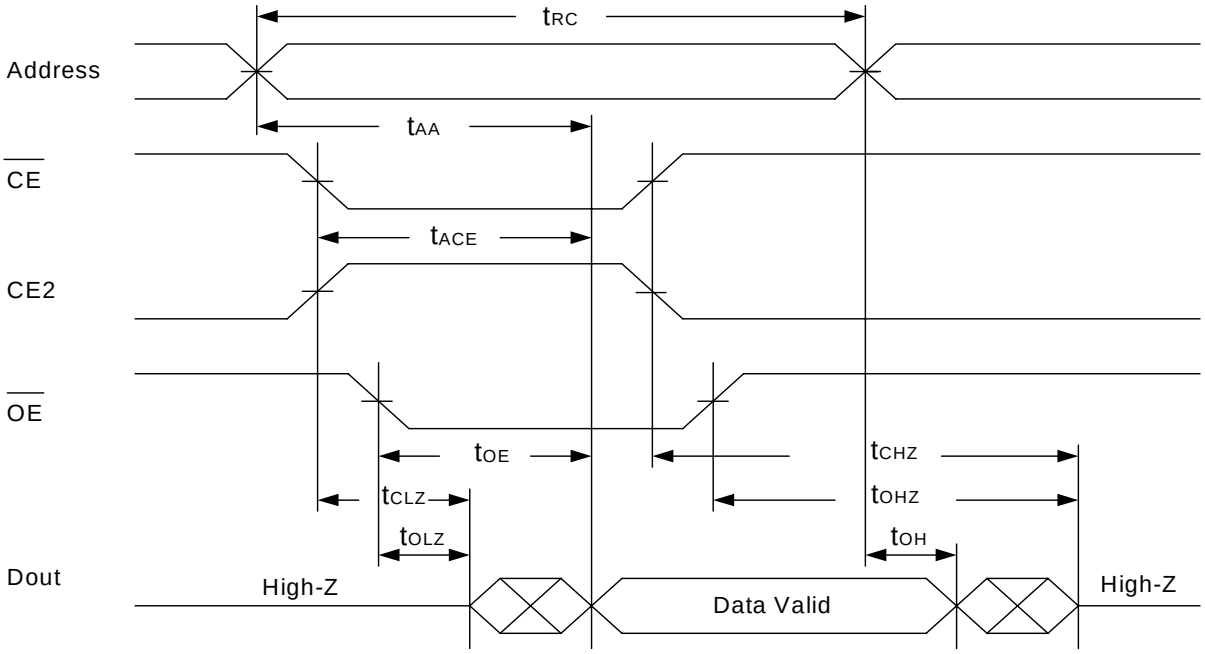
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



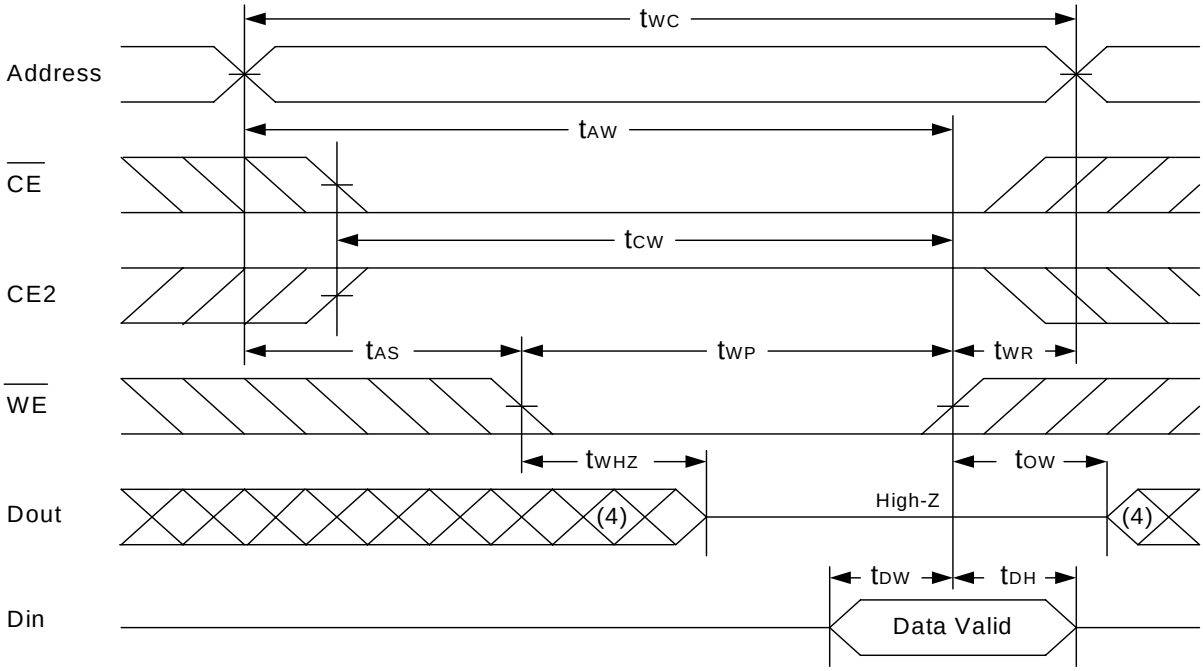
READ CYCLE 2 ($\overline{CE}$ and CE2 and $\overline{OE}$ Controlled) (1,3,4,5)



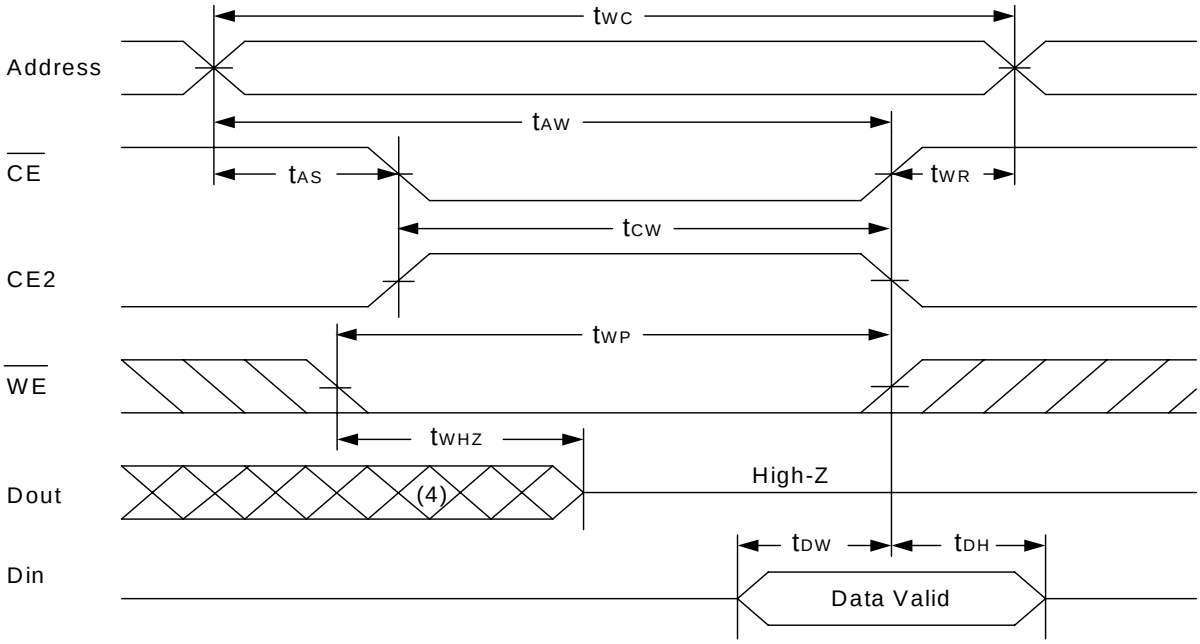
Notes :

1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected $\overline{OE}$ =low, $\overline{CE}$ =low, CE2=high.
3. Address must be valid prior to or coincident with $\overline{CE}$ =low, CE2=high; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ}, t_{OLZ}, t_{CHZ} and t_{OHZ} are specified with C_L=5pF. Transition is measured ± 500mV from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ}, t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 ($\overline{WE}$ Controlled) (1,2,3,5,6)



WRITE CYCLE 2 ($\overline{CE}$ and CE2 Controlled) (1,2,5,6)



Notes :

1. $\overline{WE}$, $\overline{CE}$ must be high or CE2 must be low during all address transitions.
2. A write occurs during the overlap of a low $\overline{CE}$, high CE2, low $\overline{WE}$.
3. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ low, t_{WP} must be greater than $t_{WHZ}+t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition and CE2 high transition occurs simultaneously with or after $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ± 500mV from steady state.

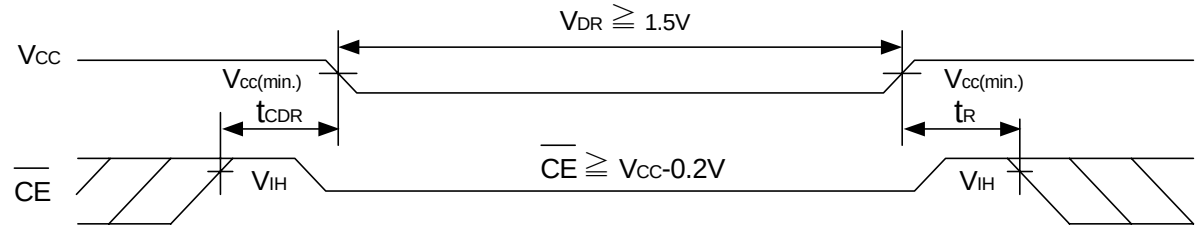
DATA RETENTION CHARACTERISTICS (T_A = 0℃ to 70℃ / -20℃ to 85℃(E))

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V_{DR}	$\overline{CE} \geqq V_{CC}$-0.2V or CE2 ≤ 0.2V		1.5	-	3.6	V
Data Retention Current	I_{DR}	Vcc=2.5V $\overline{CE} \geqq V_{CC}$-0.2V or CE2 ≤ 0.2V	-L	-	1	50	μA
			-LL	-	0.5	10	μA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)		0	-	-	ns
Recovery Time	t_R			t_{RC*}	-	-	ns

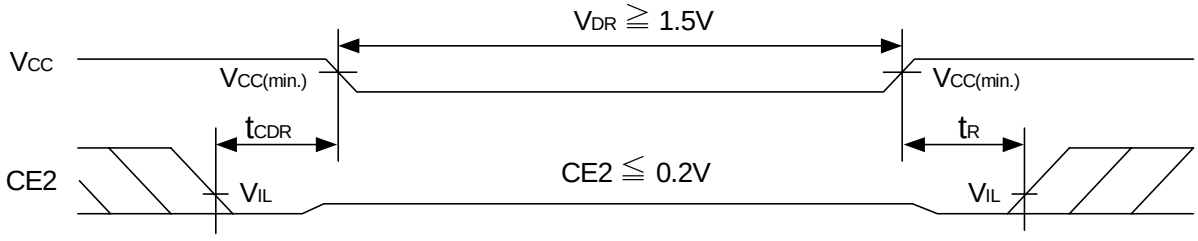
t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM

Low Vcc Data Retention Waveform (1) ($\overline{CE}$ controlled)

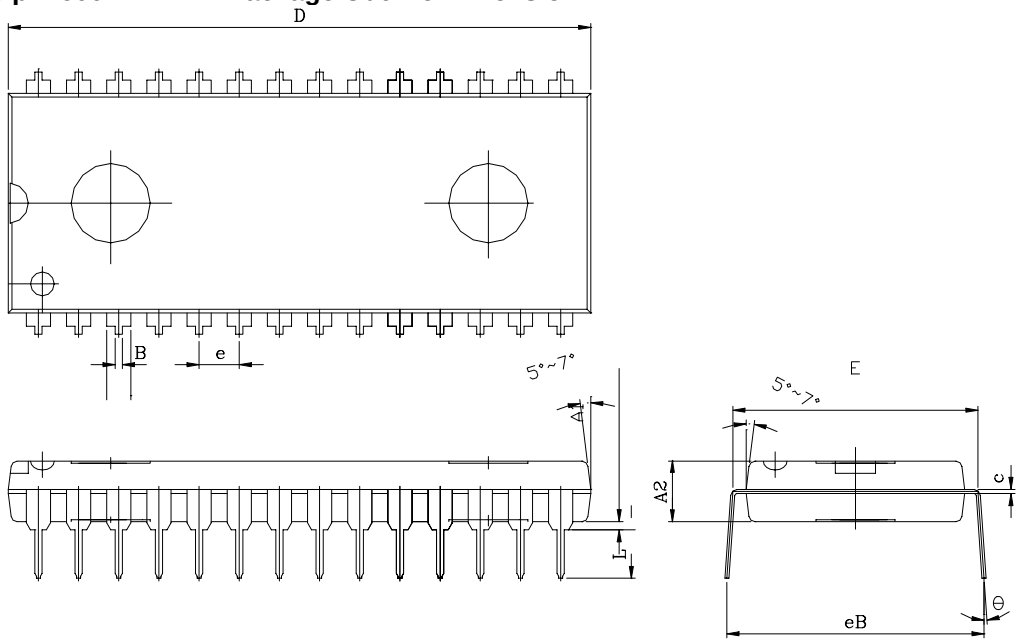


Low Vcc Data Retention Waveform (2) (CE2 controlled)



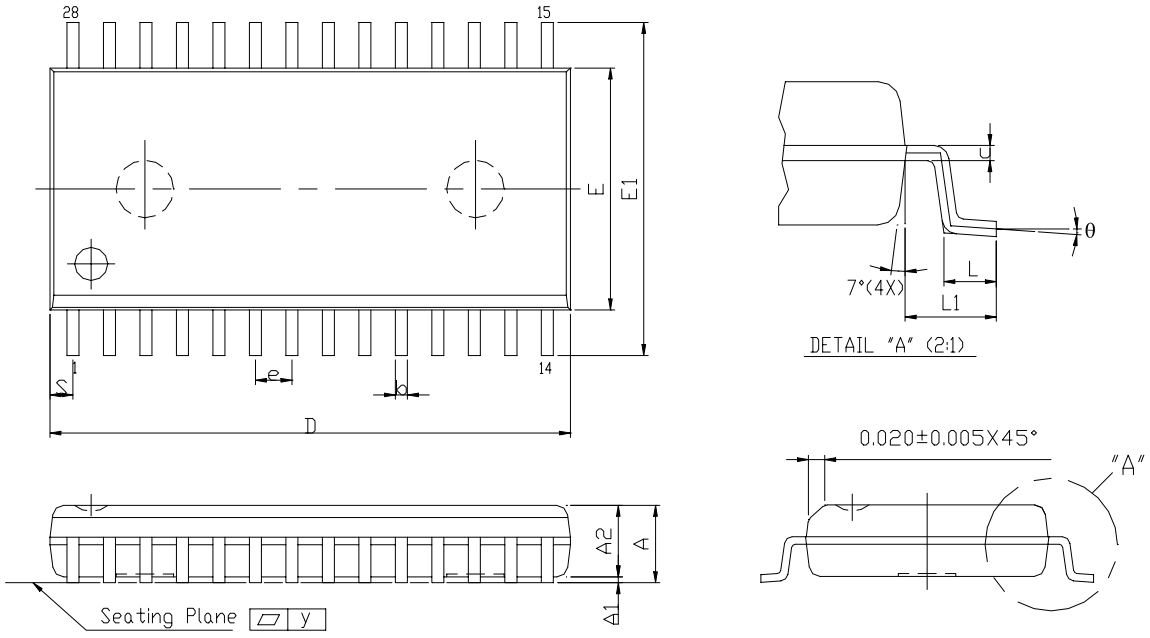
PACKAGE OUTLINE DIMENSION

28 pin 600 mil PDIP Package Outline Dimension



UNIT / SYMBOL	INCH(BASE)	MM(REF)
A1	0.010(MIN)	0.254(MIN)
A2	0.150± 0.001	3.810± 0.254
B	0.018± 0.005	0.457± 0.127
c	0.010± 0.004	0.254± 0.102
D	1.460± 0.005	37.084± 0.127
E	0.600± 0.010	15.240± 0.254
e	0.100 (TYP)	2.540(TYP)
eB	0.640± 0.03	16.256± 0.762
L	0.130± 0.010	3.302± 0.254
θ	0°~15°	0°~15°

28 pin 330 mil SOP Package Outline Dimension



UNIT / SYMBOL	INCH(BASE)	MM(REF)
A	0.112 (MAX)	2.845 (MAX)
A1	0.004(MIN)	0.102(MIN)
A2	0.098± 0.005	2.489± 0.127
b	0.016 (TYP)	0.406(TYP)
c	0.010 (TYP)	0.254(TYP)
D	0.713± 0.005	18.110± 0.127
E	0.331± 0.005	8.407± 0.127
E1	0.465± 0.012	11.811± 0.305
e	0.050 (TYP)	1.270(TYP)
L	0.0404± 0.008	1.0255± 0.203
L1	0.067± 0.008	1.702 ± 0.203
S	0.047 (MAX)	1.194 (MAX)
y	0.003(MAX)	0.076(MAX)
θ	0^o 10^o	0^o 10^o

ORDERING INFORMATION

Commerical temperature

PART NO.	ACCESS TIME(ns)	STANDBY CURRENT (μA) (TYP.)	PACKAGE
UT62L64CPC-35	35	1.5mA	28 PIN PDIP
UT62L64CPC-35L	35	1μA	28 PIN PDIP
UT62L64CPC-35LL	35	0.5μA	28 PIN PDIP
UT62L64CPC-70	70	1.5mA	28 PIN PDIP
UT62L64CPC-70L	70	1μA	28 PIN PDIP
UT62L64CPC-70LL	70	0.5μA	28 PIN PDIP
UT62L64CSC-35	35	1.5mA	28 PIN SOP
UT62L64CSC-35L	35	1μA	28 PIN SOP
UT62L64CSC-35LL	35	0.5μA	28 PIN SOP
UT62L64CSC-70	70	1.5mA	28 PIN SOP
UT62L64CSC-70L	70	1μA	28 PIN SOP
UT62L64CSC-70LL	70	0.5μA	28 PIN SOP

Extended temperature

PART NO.	ACCESS TIME(ns)	STANDBY CURRENT (μA) (TYP.)	PACKAGE
UT62L64CPC-35E	35	1.5mA	28 PIN PDIP
UT62L64CPC-35LE	35	1μA	28 PIN PDIP
UT62L64CPC-35LLE	35	0.5μA	28 PIN PDIP
UT62L64CPC-70E	70	1.5mA	28 PIN PDIP
UT62L64CPC-70LE	70	1μA	28 PIN PDIP
UT62L64CPC-70LLE	70	0.5μA	28 PIN PDIP
UT62L64CSC-35E	35	1.5mA	28 PIN SOP
UT62L64CSC-35LE	35	1μA	28 PIN SOP
UT62L64CSC-35LLE	35	0.5μA	28 PIN SOP
UT62L64CSC-70E	70	1.5mA	28 PIN SOP
UT62L64CSC-70LE	70	1μA	28 PIN SOP
UT62L64CSC-70LLE	70	0.5μA	28 PIN SOP

ORDERING INFORMATION (for lead free product)

Commerical temperature

PART NO.	ACCESS TIME(ns)	STANDBY CURRENT (μA) (TYP.)	PACKAGE
UT62L64CPCL-35	35	1.5mA	28 PIN PDIP
UT62L64CPCL-35L	35	1μA	28 PIN PDIP
UT62L64CPCL-35LL	35	0.5μA	28 PIN PDIP
UT62L64CPCL-70	70	1.5mA	28 PIN PDIP
UT62L64CPCL-70L	70	1μA	28 PIN PDIP
UT62L64CPCL-70LL	70	0.5μA	28 PIN PDIP
UT62L64CSCL-35	35	1.5mA	28 PIN SOP
UT62L64CSCL-35L	35	1μA	28 PIN SOP
UT62L64CSCL-35LL	35	0.5μA	28 PIN SOP
UT62L64CSCL-70	70	1.5mA	28 PIN SOP
UT62L64CSCL-70L	70	1μA	28 PIN SOP
UT62L64CSCL-70LL	70	0.5μA	28 PIN SOP

Extended temperature

PART NO.	ACCESS TIME(ns)	STANDBY CURRENT (μA) (TYP.)	PACKAGE
UT62L64CPCL-35E	35	1.5mA	28 PIN PDIP
UT62L64CPCL-35LE	35	1μA	28 PIN PDIP
UT62L64CPCL-35LLE	35	0.5μA	28 PIN PDIP
UT62L64CPCL-70E	70	1.5mA	28 PIN PDIP
UT62L64CPCL-70LE	70	1μA	28 PIN PDIP
UT62L64CPCL-70LLE	70	0.5μA	28 PIN PDIP
UT62L64CSCL-35E	35	1.5mA	28 PIN SOP
UT62L64CSCL-35LE	35	1μA	28 PIN SOP
UT62L64CSCL-35LLE	35	0.5μA	28 PIN SOP
UT62L64CSCL-70E	70	1.5mA	28 PIN SOP
UT62L64CSCL-70LE	70	1μA	28 PIN SOP
UT62L64CSCL-70LLE	70	0.5μA	28 PIN SOP

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