



## Matched N-Channel JFET Pairs

PRODUCT SUMMARY					
Part Number	$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ Min (V)	$g_{fs}$ Min (mS)	$I_G$ Typ (pA)	$ V_{GS1} - V_{GS2} $ Max (mV)
2N5564	-0.5 to -3	-40	7.5	-3	5
2N5565	-0.5 to -3	-40	7.5	-3	10
2N5566	-0.5 to -3	-40	7.5	-3	20

### FEATURES

- Two-Chip Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 3 pA
- Low Noise: 12 nV/√Hz @ 10 Hz
- Good CMRR: 76 dB
- Minimum Parasitics

### BENEFITS

- Tight Differential Match vs. Current
- Improved Op Amp Speed, Settling Time Accuracy
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signals
- Maximum High Frequency Performance

### APPLICATIONS

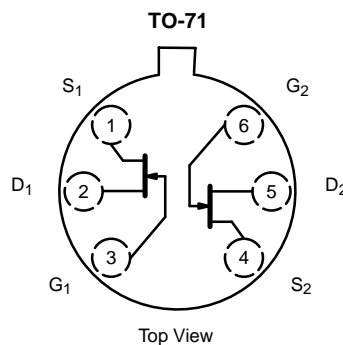
- Wideband Differential Amps
- High-Speed, Temp-Compensated, Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters
- Matched Switches

### DESCRIPTION

The 2N5564/5565/5566 are matched pairs of JFETs mounted in a TO-71 package. This two-chip design reduces parasitics for good performance at high frequency while ensuring extremely tight matching. This series features high breakdown voltage ( $V_{(BR)DSS}$  typically > 55 V), high gain (typically > 9 mS), and <5 mV offset between the two die.

The hermetically-sealed TO-71 package is available with full military processing (see Military Information).

For similar products see the low-noise U/SST401 series, and the low-leakage 2N5196/5197/5198/5199 data sheets.



### ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage	-40 V
Gate-Gate Voltage	±80 V
Gate Current	50 mA
Lead Temperature ( $1/16$ " from case for 10 sec.)	300 °C
Storage Temperature	-65 to 200 °C

Operating Junction Temperature	-55 to 150 °C
Power Dissipation :	Per Side <sup>a</sup> 325 mW
	Total <sup>b</sup> 650 mW

#### Notes

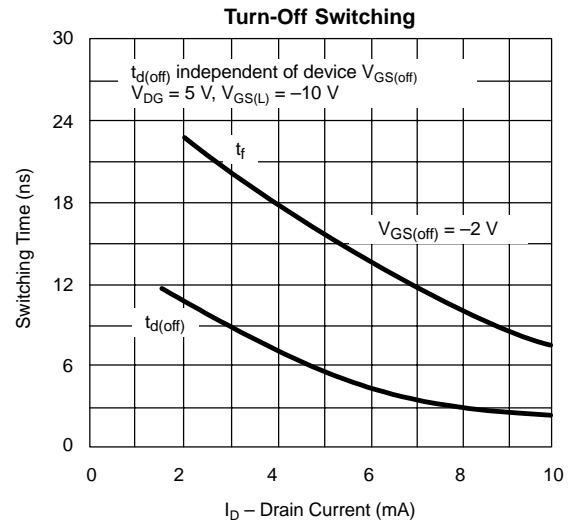
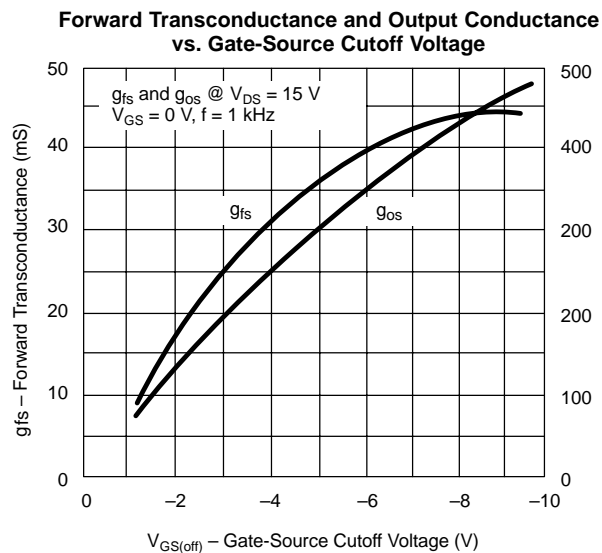
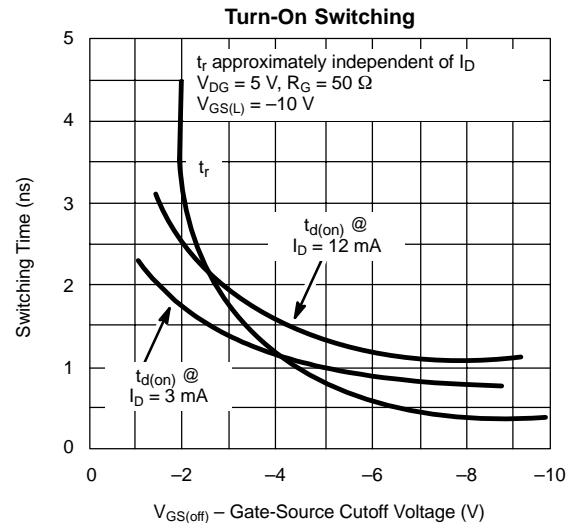
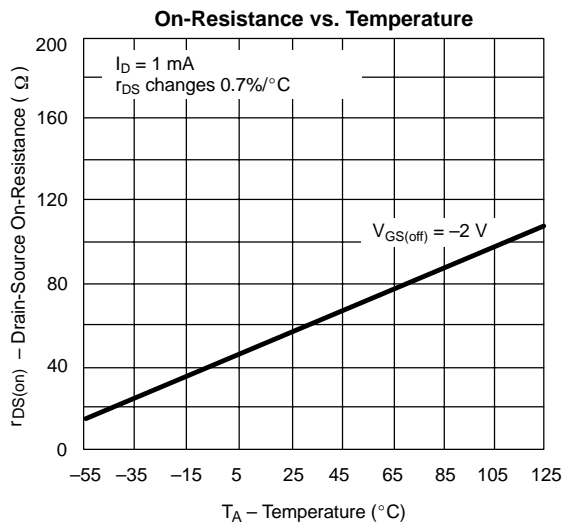
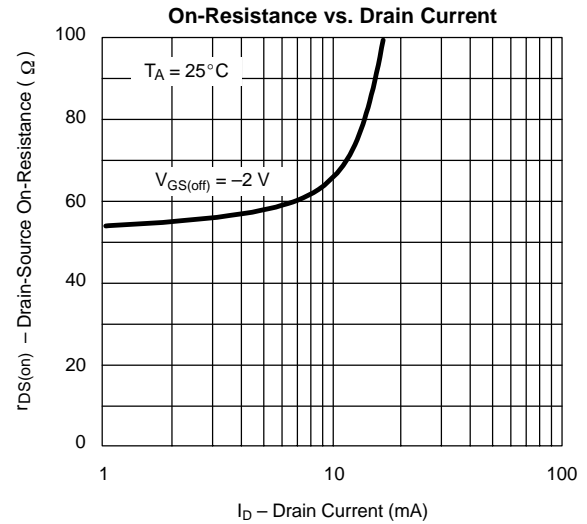
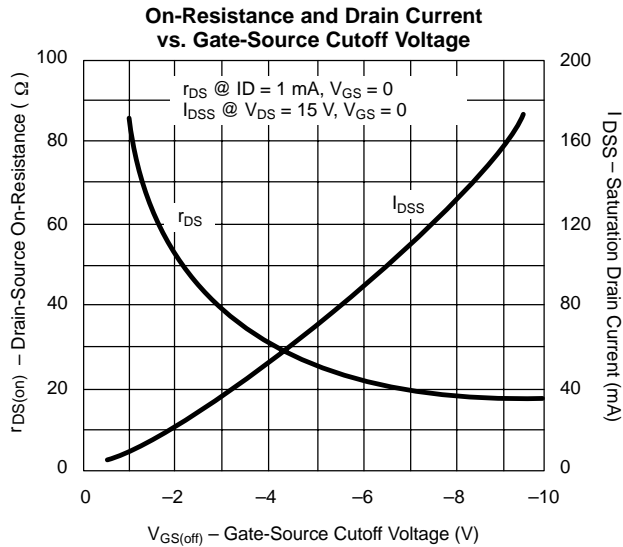
- Derate 2.6 mW/°C above 25 °C
- Derate 5.2 mW/°C above 25 °C

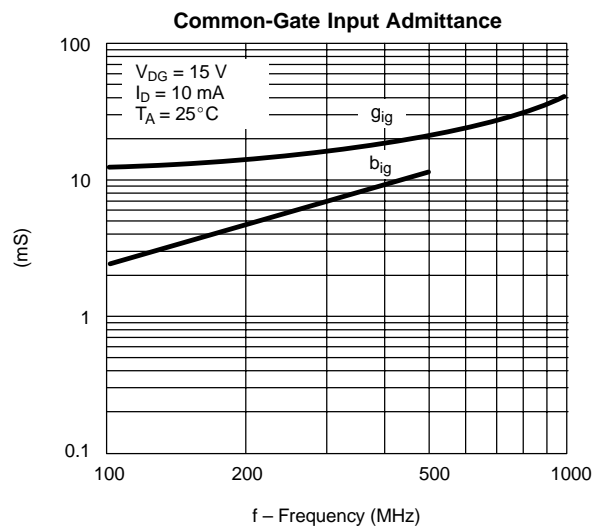
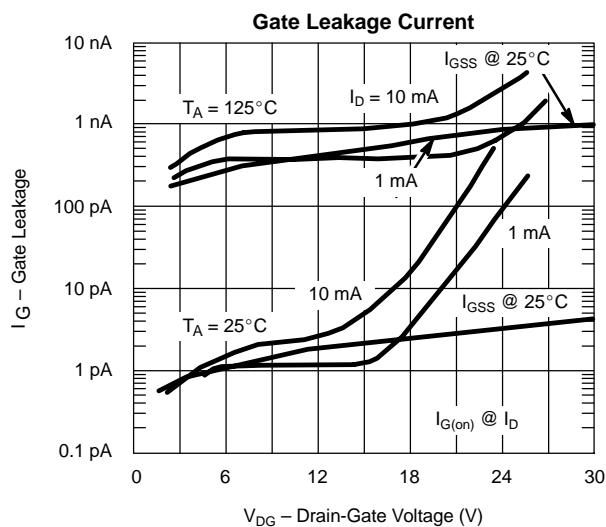
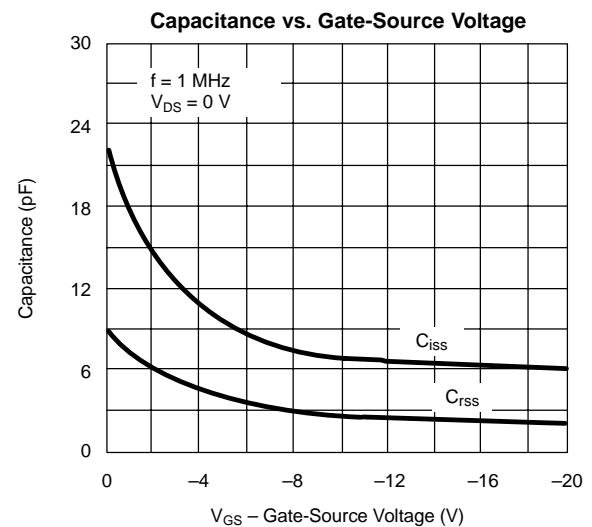
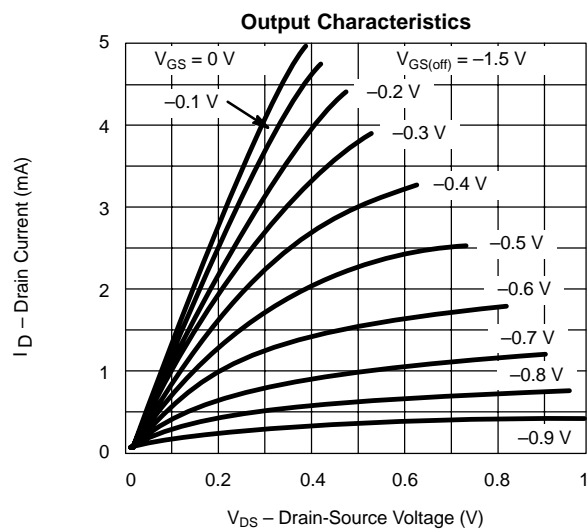
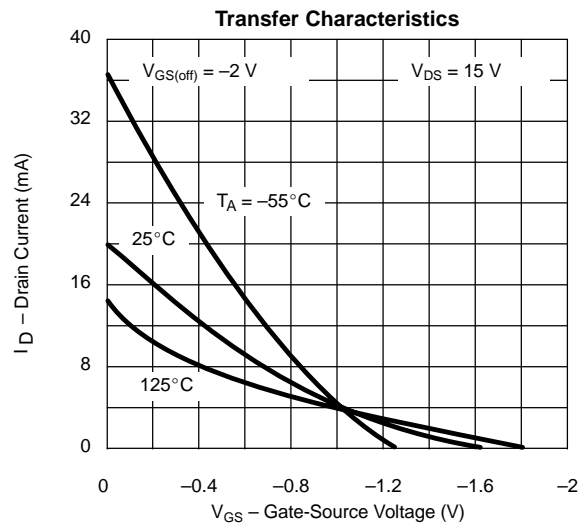
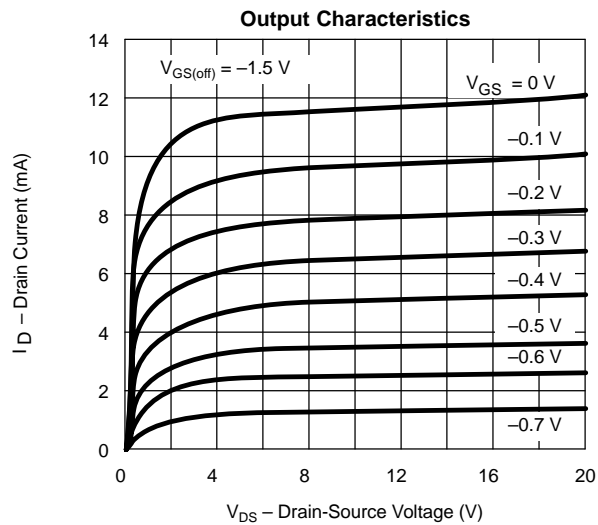
SPECIFICATIONS (T <sub>A</sub> = 25° C UNLESS OTHERWISE NOTED)										
Parameter	Symbol	Test Conditions	Typ <sup>a</sup>	Limits						Unit
				2N5564		2N5565		2N5566		
				Min	Max	Min	Max	Min	Max	
Static										
Gate-Source Breakdown Voltage	V <sub>(BR)GSS</sub>	I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0 V	-55	-40		-40		-40		V
Gate-Source Cutoff Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1 nA	-2	-0.5	-3	-0.5	-3	-0.5	-3	
Saturation Drain Current <sup>b</sup>	I <sub>DSS</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V	20	5	30	5	30	5	30	mA
Gate Reverse Current	I <sub>GSS</sub>	V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0 V	-5		-100		-100		-100	pA
		T <sub>A</sub> = 150°C	-10		-200		-200		-200	nA
Gate Operating Current <sup>c</sup>	I <sub>G</sub>	V <sub>DG</sub> = 15 V, I <sub>D</sub> = 2 mA	-3							pA
		T <sub>A</sub> = 125°C	-1							nA
Drain-Source On-Resistance	r <sub>DS(on)</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA	50		100		100		100	Ω
Gate-Source Voltage <sup>c</sup>	V <sub>GS</sub>	V <sub>DG</sub> = 15 V, I <sub>D</sub> = 2 mA	-1.2							V
Gate-Source Forward Voltage	V <sub>GS(F)</sub>	I <sub>G</sub> = 2 mA , V <sub>DS</sub> = 0 V	0.7		1		1		1	
Dynamic										
Common-Source Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 2 mA f = 1 kHz	9	7.5	12.5	7.5	12.5	7.5	12.5	mS
Common-Source Output Conductance	g <sub>os</sub>		35		45		45		45	μS
Common-Source Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 2 mA f = 100 MHz	8.5	7		7		7		mS
Common-Source Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 2 mA f = 1 MHz	10		12		12		12	pF
Common-Source Reverse Transfer Capacitance	C <sub>rss</sub>		2.5		3		3		3	
Equivalent Input Noise Voltage	e <sub>n</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 2 mA f = 10 Hz	12		50		50		50	nV/ √Hz
Noise Figure	NF	R <sub>G</sub> = 10 MΩ			1		1		1	dB
Matching										
Differential Gate-Source Voltage	V <sub>GS1</sub> -V <sub>GS2</sub>	V <sub>DG</sub> = 15 V, I <sub>D</sub> = 2 mA			5		10		20	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta V_{GS1}-V_{GS2} }{\Delta T}$	V <sub>DG</sub> = 15 V, I <sub>D</sub> = 2 mA T <sub>A</sub> = -55 to 125°C			10		25		50	μV/ °C
Saturation Drain Current Ratio <sup>c</sup>	$\frac{I_{DSS1}}{I_{DSS2}}$	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V	0.98	0.95	1	0.95	1	0.95	1	
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 2 mA f = 1 kHz	0.98	0.95	1	0.90	1	0.90	1	
Common Mode Rejection Ratio <sup>c</sup>	CMRR	V <sub>DG</sub> = 10 to 20 V I <sub>D</sub> = 2 mA	76							dB

## Notes

- a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.  
b. Pulse test: PW ≤ 300 μs duty cycle ≤ 3%.  
c. This parameter not registered with JEDEC.

NCBD

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